United States District Court,
E.D. Texas, Sherman Division.

FREESCALE SEMICONDUCTOR, INC,
Plaintiff.
v.
PROMOS TECHNOLOGIES, INC,
Defendant.

Civil Action No. 4:06-CV-491

June 19, 2008.

Background: Semiconductor manufacturer brought patent infringement action against competitor alleging infringement of three patents. Parties sought claim construction.

Holdings: Following Markman hearing, the District Court, Richard A. Schell, J., held that:
(1) term "signal termination" meant connecting an impedance located within a communication device to the receiving end of a transmission line or bus to reduce the reflection of signals when the communication device is receiving data from that transmission line or bus;
(2) term "data processing system" meant system that performs operations on data;
(3) term "data unit" meant circuitry that stores or otherwise processes data;
(4) term "enable signal" meant control signal that, when asserted, allows an operation to occur; and
(5) term "partially parallel connection" meant some of the physically separated termination circuits in the dynamic termination circuitry are connected in parallel.

Claims construed.

5,367,494, 5,467,455, 5,476,816. Construed.

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CLAIM CONSTRUCTION ORDER

RICHARD A. SCHELL**, District Judge.**

After considering the asserted patents, their respective prosecution histories, and the submissions and the arguments of counsel, the court issues the following order concerning claim construction issues:

I. INTRODUCTION

Plaintiff Freescale Semiconductor, Inc. ("Freescale") accuses defendant ProMOS Technologies, Inc. ("ProMOS") of infringing claims of three United States patents: (1) U.S. Patent No. 5,467,455 ("the '455 patent"), entitled Data Processing System and Method for Performing Dynamic Bus Termination; (2) U.S. Patent No. 5,476,816 ("the '816 patent"), entitled Process for Etching an Insulating Layer After a Metal Etching Step; and (3) U.S. Patent No. 5,367,494 ("the '494 patent"), entitled Randomly Accessible Memory Having Time Overlapping Memory Accesses. Freescale alleges infringement of claims 1-3, 6-8, 22-24, and 26-28 of the '455 patent, claims 1-4, 6-9, and 11-21 of the ' 816 patent, and claims 9-11 of the '494 patent. This order resolves the parties' various claim construction disputes.

II. GENERAL PRINCIPLES OF CLAIM CONSTRUCTION

[1] [2] "A claim in a patent provides the metes and bounds of the right which the patent confers on the patentee to exclude others from making, using or selling the protected invention." Burke, Inc. v. Bruno Indep. Living Aids, Inc., 183 F.3d 1334, 1340 (Fed.Cir.1999). Claim construction is an issue of law for the court to decide. Markman v. Westview Instruments, Inc., 52 F.3d 967, 970-71 (Fed.Cir.1995) (en banc).

[3] [4] [5] To ascertain the meaning of claims, the court looks to three primary sources: the claims, the specification, and the prosecution history. Markman, 52 F.3d at 979. A patent's claims must be read in view of the specification, of which they are a part. Id. Under 35 U.S.C. s. 112, the specification must contain a written description of the invention that enables one of ordinary skill in the art to make and use the invention. For claim construction purposes, the description may act as a sort of dictionary, which explains the invention and may define terms used in the claims. Markman, 52 F.3d at 979.

[6] Nonetheless, it is the function of the claims, not the specification, to set forth the limits of the patentee's claims. Otherwise, there would be no need for claims. SRI Int'l v. Matsushita Elec. Corp., 775 F.2d 1107, 1121 (Fed.Cir.1985) (en banc). The patentee is free to be his own lexicographer, but any special definition given to a word must be clearly set forth in the specification. Intellicall, Inc. v. Phonometrics, 952 F.2d 1384, 1388 (Fed.Cir.1992). And, although the specification may indicate that certain embodiments are preferred, particular embodiments appearing in the specification will not be read into the claims when the claim language is broader than the embodiments. Electro Med. Sys., S.A. v. Cooper Life Sciences, Inc., 34 F.3d 1048, 1054 (Fed.Cir.1994).

The court's claim construction analysis is informed by the Federal Circuit's decision in Phillips v. AWH Corporation, 415 F.3d 1303 (Fed.Cir.2005) (en banc). In Phillips, the court set forth several guideposts that courts should follow when construing claims. In particular, the court reiterated that "the claims of a patent define the invention to which the patentee is entitled the right to exclude." 415 F.3d at 1312 (emphasis added) (quoting Innova/Pure Water, Inc. v. Safari Water Filtration Systems, Inc., 381 F.3d 1111, 1115 (Fed.Cir.2004)). To that end, the words used in a claim are generally given their ordinary and customary meaning. Id. The ordinary and customary meaning of a claim term "is the meaning that the term would have

to a person of ordinary skill in the art in question at the time of the invention, *i.e.*, as of the effective filing date of the patent application." Id. at 1313.

The primacy of claim terms notwithstanding, Phillips made clear that "the person of ordinary skill in the art is deemed to read the claim term not only in the context of the particular claim in which the disputed term appears, but in the context of the entire patent, including the specification." Id. Although the claims themselves may provide guidance as to the meaning of particular terms, those terms are part of "a fully integrated written instrument." Id. at 1315 (quoting Markman, 52 F.3d at 978). Thus, Phillips emphasized the specification as being the primary basis for construing the claims. Id. at 1314-17. The construction that stays true to the claim language and most naturally aligns with the patent's description of the invention will be, in the end, the correct construction. Consequently, Phillips emphasized the important role the specification plays in the claim construction process.

The prosecution history also plays an important role in claim interpretation. The prosecution history helps to demonstrate how the inventor and the PTO understood the patent. Phillips, 415 F.3d at 1317. Because the file history, however, "represents an ongoing negotiation between the PTO and the applicant," it may lack the clarity of the specification and thus be less useful in claim construction proceedings. Id. Nevertheless, the prosecution history is intrinsic evidence and is relevant to determining how the inventor understood the invention and whether the inventor limited the invention during prosecution by narrowing the scope of the claims.

Phillips rejected a claim construction approach that sacrificed the intrinsic record in favor of extrinsic evidence, such as dictionary definitions or expert testimony. The *en banc* court condemned the suggestion made by Texas Digital Systems, Inc. v. Telegenix, Inc., 308 F.3d 1193 (Fed.Cir.2002), that a court should discern the ordinary meaning of the claim terms (through dictionaries or otherwise) before resorting to the specification for certain limited purposes. Id. at 1319-24. According to Phillips, reliance on dictionary definitions at the expense of the specification had the effect of "focus[ing] the inquiry on the abstract meaning of words rather than on the meaning of the claim terms within the context of the patent." Id. at 1321. Phillips did not, however, preclude all use of dictionaries in claim construction proceedings. Instead, the court assigned dictionaries a role subordinate to the intrinsic record. Id. at 1323-25.

With these principles in mind, the court now turns to a discussion of the relevant claim terms.

III. THE '455 PATENT

1. Background of the Technology

In general, the '455 patent describes circuitry designed both to reduce unwanted signal reflection at the transmitting end of a bi-directional bus and to conserve power. The system and method described in the '455 patent enable selected termination circuitry only when data is being received from a bus, and disable the termination circuitry when data is not being received from a bus. The selective enabling and disabling of the termination circuitry allows the system to reduce unwanted signal reflection while also conserving power.

2. Agreed Constructions

The parties have agreed that "coupled to" in claim 1 means "electrically connected to," and that "coupled between" in claim 22 means "electrically connected between." FN1

FN1. Though the parties briefed other proposed constructions for "coupled between," they agreed at the Markman hearing that this term means "electrically connected between."

3. Disputed Constructions

The parties originally disputed the construction of 14 terms of the '455 patent. They have since agreed to the construction of "coupled between," as described above. The parties agreed to address only five of the disputed terms at the Markman hearing and to rely on the briefing alone for the remaining nine disputed terms. The court will construe the terms addressed at the hearing first.

Claims 1 and 22 of the '455 patent are representative of how the disputed claims terms are used in the asserted claims. Claim 1 of the '455 patent is an independent apparatus claim. It provides:

A data processing system having a communication device, the communication device being an integrated circuit having a plurality of external pins, the plurality of external pins being coupled to receive data from external to the communication device and transmit data external to the communication device, the communication device comprising:

circuitry for signal termination having a plurality of first input/output terminals coupled to the plurality of external pins via a plurality of data lines, the circuitry for signal termination having a second input/output terminal for providing data to or receiving data from internal to the communication device, the circuitry for signal termination having an input for receiving an enable signal from either internal or external to the communication device and having a termination component, the enable signal allowing the circuitry for signal termination to couple the termination component to the plurality of external pins when the enable signal is asserted and decoupling the termination component from the plurality of external pins when the enable signal is deasserted.

Claim 22 of the '455 patent is also an independent apparatus claim. It provides, in part:

An integrated circuit having a terminal for communicating parallel binary data, the integrated circuit comprising:

a data unit for storing and manipulating the data within the integrated circuit; dynamic termination circuitry coupled between the data unit and the terminal for communicating parallel binary data, the dynamic termination circuitry having N physically separated termination circuits....

a. Signal Termination (Claims 1, 2)

[7] The first term for construction is "signal termination." Freescale proposes "connecting an impedance located within a communication device to the receiving end of a transmission line or bus to reduce the effects of signal reflection when the communication device is receiving data from that transmission line or bus." ProMOS proposes "a load that substantially eliminates reflections of signals received from a transmission line or bus." There are two main disputes: (1) whether "impedance" or "load" should be used in this construction and (2) whether signal reflections must be "substantially eliminated" or simply "reduced."

Because the specification uses the term impedance-and not the term load-when referring to circuitry for

signal termination, the term impedance should be used in this construction. For example, the specification describes that, in a preferred embodiment, "[t]he termination circuit contains one or more circuit components which when coupled to the data line reduce reflection or change line impedance on the bi-directional external bus 17 when data is being received by the device 10." '455 patent, 4:28-32; *see also* id. at 1:21; 5:16-19; 7:56-58; and 8:21-26. Moreover, the parties were unable to articulate a meaningful distinction between these two terms at the Markman hearing. There is thus no compelling reason to depart from the terminology used in the patent in construing this term.

While there are two instances where the patentee used the phrase "avoid signal reflection" in the specification, there are approximately 15 instances where the patentee describes the invention's objective of reducing signal reflection. *See* '455 patent, Abstract; 1:23-26; 1:52-57; 2:55-59; 4:28-32; 6:2-7; 6:43-45; 6:60-62; 7:23-27; 7:53-58; 7:58-60; 8:32-38; 9:7-8; 9:16-18; and 9:55-58. The specification does not use the term "substantially eliminates" (as proposed by ProMOS), a term that would inject unnecessary ambiguity into this construction and that is not grounded in the intrinsic record.

ProMOS appears to temper the word "avoid" found in its specification citations (implying that signal reflections are eliminated entirely) by using "substantially eliminates" in its proposed construction. In support of its proposal, ProMOS argues that signal termination would mean substantial elimination of signal reflections to a person of ordinary skill in the art. It did not, however, submit any evidence supporting such an understanding during briefing or at the Markman hearing. In light of the intrinsic record and lack of extrinsic evidence supporting ProMOS's proposed construction, the court finds that this term alone, as viewed by a person of ordinary skill in the art in light of the specification, does not require substantial elimination of signal reflection.

The court also finds that the invention is designed to reduce the actual reflection of signals rather than the effect of signal reflection, as proposed by Freescale. Freescale did not cite any intrinsic support for broadening this term to include both reducing signal reflection and reducing the effects of signal reflection, so the court declines to adopt this portion of its proposed construction.

Due to the specification's consistent use of the term "impedance," and its consistent explanation of the invention's ability to reduce signal reflection, this term means "connecting an impedance located within a communication device to the receiving end of a transmission line or bus to reduce the reflection of signals when the communication device is receiving data from that transmission line or bus."

b. Dynamic Termination Circuitry (Claim 22)

[8] Freescale proposes that "dynamic termination circuitry" means "signal termination circuitry that may be selectively coupled or decoupled in response to an enable signal." FN2 ProMOS proposes that this term means "circuitry for signal termination that is selectively enabled or disabled on the fly as determined by a control signal indicating the direction of data signals on the bus." FN3 The parties' dispute concerning this construction boils down to two issues: (1) whether to include "on the fly" and (2) whether the enable signal indicates the direction of data signals on the bus. "On the fly" is not used in the patent and is vague and ambiguous. The ' 455 patent describes a mechanism for detecting data direction and enabling or disabling the termination circuitry in response, without reference to specific response time. Inclusion of "on the fly" would be unhelpful to a jury and adds a limitation that does not appear in the claims or in the specification.

FN2. At the Markman hearing, Freescale agreed to "circuitry for signal termination that is selectively

enabled or disabled in response to an enable signal."

FN3. At the Markman hearing, ProMOS agreed to the inclusion of "enable signal" rather than "control signal" in its proposed construction.

The parties' second dispute appears to be whether the enable signal itself must indicate the direction of data signals on the bus. As described in the ' 455 patent, an enable signal is asserted only in the event that data is incoming to the memory device. *See, e.g.,* '455 patent, 1 :53-57. Assertion of the enable signal, therefore, is based, at least in part, on the direction of data signals on the bus. The patent provides for the possibility that a variety of control signals may be used to form a termination enable signal. ' 455 patent, 3 :10-18. In other words, the patent specifically provides that enable signals may be control signals other than read/write signals (not all of which directly indicate the direction of data signals on the bus), so the enable signal itself need not contain information directly indicating the direction of data signals on the bus. However, its assertion must be based, at least in part, on the direction of data signals on the bus.

The term "dynamic termination circuitry," therefore, means "circuitry for signal termination that is selectively enabled or disabled in response to an enable signal whose assertion is based, at least in part, on the direction of data signals on the bus."

c. Terminal for Communicating Parallel Binary Data (Claims 22, 26)

[9] Freescale argues that this term does not need to be construed or, alternatively, that it should be construed to mean "connections for communicating parallel binary data." ProMOS argues that this term is indefinite or, alternatively, that it should be construed to mean "a single connection point in a system that communicates parallel binary information."

[10] [11] [12] Under 35 U.S.C. s. 112, para. 2, claims must "particularly point[ ] out and distinctly claim[ ] the subject matter which the applicant regards as his invention." If the patentee does not comply with this obligation, the claim or claims that fail to particularly point out and distinctly claim the subject matter are invalid as indefinite. A claim is indefinite if, when read in light of the specification, it does not reasonably apprise those skilled in the art of the scope of the claim. Allen Eng'g Corp. v. Bartell Indus., Inc., 299 F.3d 1336, 1348-49 (Fed.Cir.2002). "The standard of indefiniteness is somewhat high; a claim is not indefinite merely because its scope is not ascertainable from the face of the claims." Amgen, Inc. v. Hoechst Marion Roussel, Inc., 314 F.3d 1313, 1342 (Fed.Cir.2003). Rather, a claim is indefinite under s. 112, para. 2 only if it is "insolubly ambiguous, and no narrowing construction can properly be adopted." Exxon Research & Eng'g Co. v. United States, 265 F.3d 1371, 1375 (Fed.Cir.2001).

ProMOS presented no evidence during briefing or at the Markman hearing that a person of ordinary skill in the art would be unable to understand the scope of the claims containing this term. Indeed, its alternate proposed construction reveals that there is at least some possible construction that would prevent a finding that this claim term is "insolubly ambiguous." ProMOS argues that the word "terminal" means a single connection point and that "communicating parallel binary data" necessarily requires more than a single connection point. Beginning with the assumption that its alternative proposed construction is correct, ProMOS argues that it is impossible to communicate data in parallel through a single point and that the claim is thus indefinite. This argument, however, is more accurately described as an enablement argument

under 35 U.S.C. s. 112, para. 1: that the '455 patent does not enable a person skilled in the art to make and use the invention. The court finds that ProMOS's indefiniteness argument lacks merit and that this term should be construed.

Figure 1 of the '455 patent and the "Summary of the Invention" section of the specification resolve the parties' dispute. The specification states that "[t]he circuitry for terminating has a first input/output terminal coupled to the at least one external pin via at least one data line." '455 patent, 1 :64-66. In other words, a single terminal may be coupled to more than one external pin; a terminal is not limited to a single connection point. This construction is confirmed by Figure 1, which shows a single terminal at each end of the bi-directional bus 17. Each of the terminals is labeled "PINS," illustrating-consistent with 1:64-66-that a single terminal may be associated with multiple pins (i.e., multiple connections). Because a single terminal may be comprised of multiple connections, Freescale's proposed construction is correct.

The term "terminal for communicating parallel binary data" means "connections for communicating parallel binary data."

d. Optimal Impedance (Claim 28)

[13] Freescale argues that this term means "one impedance among a plurality of possible impedances." ProMOS argues that this term means "for a given system, the best impedance as determined by reducing reflections on a transmission line or bus."

Freescale argues that the patentee acted as his own lexicographer with respect to this term in claim 28. However, its proposed construction renders the word "optimal" meaningless and ignores additional qualifying language in claim 28. The entire phrase from claim 28 upon which Freescale relies states: "the optimal impedance being one impedance among a plurality of possible impedances *where each possible impedance is capable of being provided by the circuitry*." '455 patent, 13 :25-14 :1 (emphasis added). In other words, the patentee clarified that the optimal impedance is not the single theoretical best impedance; rather, it is the best impedance selected from a finite set of possible impedances within a given device.

ProMOS's proposed construction is consistent with the intrinsic record, although it will be helpful for the jury to clarify that a given system has a predetermined, finite set of possible impedances. The term "optimal impedance" means "the best impedance, selected from among a plurality of possible impedances within a given system, for reducing signal reflections on a transmission line or bus."

e. Data Processing System

[14] Freescale argues that this term does not need to be construed or, alternatively, that it means "system that performs operations on data." ProMOS argues that this term means "system that performs processing, storage, and other operations on data." The parties thus agree that a data processing system performs operations on data. The parties dispute, however, whether those operations *must* include at least processing, storage, and "other operations."

As described in the '455 patent, FIG. 1 illustrates a data processing system. '455 patent, 3 :65. The data processing system of FIG. 1 has a device 10 and device 12, each of which is an integrated circuit. Id. at 3:66-4:2. As the specification explains, although device 10 and device 12 are analogous as illustrated in FIG. 1, they may be very different devices. Id. at 4:56-60. For example, either device 10 or device 12 may be, among other things, a memory device (such as a DRAM), a peripheral device, a microprocessor, or a central

processing unit (CPU). Id. at 4:2-14. Devices 10 and 12, therefore, may or may not be the same type of device, and the types of devices that may comprise the data processing system-and the operations they perform-thus vary considerably.

Freescale's proposed construction takes this data processing system device and functional variability into account. For example, if devices 10 and 12 are a peripheral device and a CPU, the operations performed on data may be different from the operations performed by a DRAM and a microprocessor. While some combinations of devices may perform "processing, storage, and other operations," not all combinations must necessarily do so. Moreover, the phrase "and other operations" in ProMOS's proposed construction is ambiguous. For example, it is unclear how many or what "other operations" *must* be performed under ProMOS's proposed construction for a system to qualify as a data processing system.

ProMOS's proposed construction additionally relies on a dictionary definition that defines "data processing system" to mean "a system ... that performs input, processing, storage, output, and control functions to accomplish a sequence of operations." ProMOS Br. at 8. ProMOS does not explain why the court should modify this dictionary definition to include only "processing, storage, and other" undefined operations.

Regardless of the type of devices 10 and 12, the data processing system must perform operations on data. The precise operations performed, however, may vary. *See* '455 patent, 4 :2-14. Accordingly, the court construes "data processing system" to mean "system that performs operations on data."

f. Data Unit

[15] Freescale argues that "data unit" means "circuitry that stores or otherwise processes data," while ProMOS argues that it should be construed to have different meanings, depending on the claim in which it appears. ProMOS argues that, for claims 6 and 7, it means "CPU of a data processor or a memory array containing a plurality of memories," but for claim 22, it means only "CPU of a data processor." The central dispute, therefore, is whether "data unit" should be limited to the specific examples of a data unit provided in the specification and in claim 7, or whether the term encompasses a broader category of "data units."

The Federal Circuit has made clear that "[u]nless otherwise compelled, when different claims of a patent use the same language, we give that language the same effect in each claim." Innova/Pure Water, Inc. v. Safari Water Filtration Sys., 381 F.3d 1111, 1119 (Fed.Cir.2004). The court finds no compelling reason to depart from this general principle in construing this term.

[16] [17] First, ProMOS's proposed construction would render the scope of claims 6 and 7 exactly congruent. Claim 6, which depends from claim 1, requires, among other things, "a data unit internal to the communication device." '455 patent, 10:11-13. Claim 7, which also depends from claim 1, requires, among other things, "a data unit internal to the communication device wherein the data unit" is a memory array containing a plurality of memories or a CPU of a data processor. Id. at 10:14-20. The only difference between claims 6 and 7 is claim 7's use of a *Markush* group consisting of a memory array and CPU.FN4 ProMOS's proposed construction, therefore, would improperly render dependent claims 6 and 7 exactly congruent. *See* Tate Access Floors v. Maxcess Techs., 222 F.3d 958, 967-68 (Fed.Cir.2000) (acknowledging the doctrine of claim differentiation, i.e., that two claims of a patent are presumptively of different scope).

FN4. "A Markush group is a listing of specified alternatives of a group in a patent claim, typically expressed in the form: a member selected from the group consisting of A, B, and C.... It is well known that

'members of the Markush group are ... alternatively usable for the purposes of the invention.' Moreover, '[a] Markush group, incorporated in a claim, should be 'closed,' i.e. it must be characterized with the transition phrase 'consisting of,' rather than 'comprising' or 'including.' ' " Abbott Laboratories v. Baxter Pharmaceutical Products, Inc., 334 F.3d 1274, 1280-81 (Fed.Cir.2003) (citations omitted).

Second, ProMOS argues that independent claim 22 requires a "data unit for storing and manipulating data." According to ProMOS, "data unit" in claim 22 must therefore exclude a memory array because a memory does not manipulate data. ProMOS Br. at 10. The court need not decide this fact issue in construing this term. Rather than alter the definition of the general term "data unit," the subsequent claim language "for storing and manipulating data" further specifies the type of data unit required by the claim. The broader term "data unit" (as used in each of claims 6, 7, and 22) includes any circuitry that stores or otherwise processes data, while claim 7 is limited by subsequent claim language to either a memory array or CPU, and claim 22 is limited to a data unit "for storing and manipulating data."

The court thus construes the term "data unit" to mean "circuitry that stores or otherwise processes data."

g. Enable Signal

[18] Freescale argues that "enable signal" means "a control signal that, when asserted, allows the circuitry for signal termination to couple the termination component to the plurality of external pins and decouples the termination component from the plurality of external pins when it is deasserted." ProMOS argues that this term means "signal that, when asserted, allows a device to operate."

Freescale's proposed construction incorporates subsequent claim language of claim 1 (which describes what occurs when the enable signal is asserted or deasserted), thus rendering the subsequent claim language redundant and superfluous. *See, e.g.,* '455 patent, 9 :49-54. ProMOS's proposed construction, on the other hand, would potentially be confusing to a jury because the enabled "device" in claim 1 is the dynamic termination circuitry. *Id*. Indeed, inclusion of "device" in this construction may lead jurors to believe that the "enable signal" must allow device 10 (communications device) to operate-rather than allow the dynamic termination circuitry to operate, as the claim requires.

The court thus construes "enable signal" to mean "control signal that, when asserted, allows an operation to occur."

h. Read /Write Signal

Freescale argues that "read/write signal" means "control signal that indicates when the integrated circuit is being subject to a read or write operation," while ProMOS argues that it means "control signal indicating the direction of data signals on the bus, which corresponds to whether a read or write operation is performed." ProMOS characterizes the parties' dispute as whether the read/write signal must indicate the direction of data signals on the bus. ProMOS Br. at 17-18. As explained below, however, including "indicating the direction of data signals on the bus" is at least redundant and likely imports an additional limitation into this term that is clear from the context of the claim language.

Claim 28 requires a "read/write signal that indicates when the integrated circuit is being subject to a read or write operation." '455 patent, 13 :19-21. While the specification indicates that, in the preferred embodiment, the read/write signal indicates the direction of data signals on the bus (*see* ' 455 patent, 2 :59-63, 3 :22-30),

this passage simply describes the same function of the read/write signal in different terms. That is, "indicating the direction of data signals on the bus" is another way of describing "when the integrated circuit is being subject to a read or write operation." For example, if the data signals are coming into the device via the bus, the device is being subject to a write operation, and if the data signals are going out of the device, the device is being subject to a read operation. It is thus unnecessary to state the same function in two different ways in this construction.

Moreover, Freescale's proposed construction for "read/write signal" unnecessarily includes subsequent claim language, thus rendering the subsequent claim language redundant and superfluous.

The court thus finds that this term is clear as written, with subsequent claim language describing its purpose, and that neither parties' proposed construction adds clarity. The court, therefore, declines to construe this term.

i. Input/Output Terminals

[19] Freescale argues that "input/output terminals" does not need to be construed or, alternatively, that it means "connections in a system at which data can be input and output." ProMOS argues that it means "connection points at which data can be input or output or both." Because the court has determined that a terminal comprises "connections" rather than "connection points" (*see supra* Section III.3.c), and because the parties agree that this construction should include at least the possibility of input *and* output, the only remaining dispute is whether the terminal must also be able to only input *or* only output.

The parties' dispute appears to focus on whether the input/output terminal must allow data to be input and output *at the same time*. Freescale argues that a single terminal cannot allow data to be both input and output at the same time and that this construction should not require this impossibility. ProMOS disagrees. According to ProMOS, therefore, an input/output terminal must seemingly allow data to either (1) always be input (2) always be output or (3) be input and output at the same time. In other words, ProMOS appears to argue that a terminal that sometimes allows data to be input and sometimes allows data to be output would not qualify as an input/output terminal under its proposed construction. That is, the terminal must always do one or the other or both at the same time.

ProMOS's proposed construction, however, does not qualify "both" with "at the same time." As a result, neither parties' proposed construction would require that the terminal input and output at the same time. Terminals that sometimes allow data to be input and sometimes allow data to be output, as well as terminals that allow data to be input and output at the same time (if such terminals indeed exist), would qualify as input/output terminals under either parties' proposed construction. Both types of terminals would comprise "connections in a system at which data can be input and output" (Freescale) and connections "at which data can be input or output or both" (ProMOS).

ProMOS primarily relies on the phrase in which this term appears-"input/output terminals for providing data to *or* receiving data from internal to the communication device" ('455 patent, 9 :43-45 (emphasis added))-as support for its proposed construction. According to ProMOS, this claim language clarifies that the input/output terminal is always used to provide data to *or* always receive data from internal to the communication device-i.e., input or output, but not both. ProMOS, however, provides no support for such a narrow reading of the claim.

Moreover, the patentee knew how to distinguish the terms input, output, and input/output. *See* '455 patent, 6 :5-6 (referencing "output buffers, input buffers, and input/output (I/O) buffers"). If, as ProMOS argues, "input/output terminal" encompassed terminals that *only* allow data to be input or *only* allow data to be output, in addition to terminals that allow both, the term "input/output terminal" would encompass input terminals, output terminals, and input/output terminals.

The court thus construes "input/output terminal" to mean "connections in a system at which data can be input and output." Data need not be input and output through the terminal at the same time and may thus "provid[e] data to or receiv[e] data from internal to the communications device," as required by the claims.

j. Physically Separated Termination Circuits

Freescale argues that "physically separated termination circuits" means "distinct termination circuits (when the dynamic termination circuitry contains one or more termination circuits)," while ProMOS argues that it means "individual termination circuits that are physically distinct from each other."

The court finds that this term is clear on its face, and neither party provides a construction that will further aid jurors in understanding the claim. The court thus declines to construe this term.

k. "Partially Parallel Connection," "Partially Serial Connection," and "Part-Serial and Part-Parallel Connection" (Claim 24)

[20] [21] [22] ProMOS argues that each of these terms is indefinite, while Freescale argues that they can be construed. As described in Section III.3.c, *supra,* a claim is indefinite only when it is "insolubly ambiguous, and no narrowing construction can properly be adopted." Exxon Research & Eng'g Co., 265 F.3d at 1375.

Freescale argues that "partially parallel connection" means "at least some of the physically separated termination circuits in the dynamic termination circuitry can be connected in parallel," that "partially serial connection" means "at least some of the physically separated termination circuits in the dynamic termination circuitry can be connected in series," and that "part-serial and part-parallel connection" means "at least some of the physically separated terminationcircuits in the dynamic termination circuitry can be connected in series with other physically separated termination circuits, and at least some of the physically separated termination circuits in the dynamic termination circuitry can be connected in parallel with other physically separated termination circuits."

The court notes that the specification does not use the terms "partially parallel," "partially serial," or "part-serial and part-parallel." It does, however, explain that in a given system, various termination circuits can be enabled or disabled to provide a variety of different impedances. *See, e.g.,* ' 455 patent, 8 :9-54. Selectively enabled termination circuits, each providing different levels of resistance, can thus be connected serially, in parallel, or in part-serial and part-parallel to achieve the desired resistance. *Id*. Indeed, selective enabling of the appropriate termination circuitry is how optimal impedance for a given system is achieved. *See, e.g.,* '455 patent, claim 28. Because the court finds that these terms are not insolubly ambiguous, it will construe each term.

Freescale's proposed constructions include two phrases that the court declines to adopt. First, each construction begins with "at least," which could include all of the termination circuits. If all termination circuits were connected in parallel, however, the claimed "partially parallel connection" would be entirely parallel. Second, the phrase "can be connected" implies that the termination circuits need not necessarily be

connected. Thus, for a connection that claim 24 requires to be "partially parallel," for example, Freescale's proposed construction would include termination circuits that have the capability of being, but are not necessarily, connected in parallel.

For these reasons, the court construes these terms as follows:

"Partially parallel connection" means "some of the physically separated termination circuits in the dynamic termination circuitry are connected in parallel."

"Partially serial connection" means "some of the physically separated termination circuits in the dynamic termination circuitry are connected in series."

"Part-serial and part-parallel connection" means "some of the physically separated termination circuits in the dynamic termination circuitry are connected in series, while some of the physically separated termination circuits in the dynamic termination circuitry are connected in parallel."

IV. THE '494 PATENT

1. Background of the Technology

In general, the '494 patent describes a memory device that executes time overlapping memory access operations of two or more storage locations in a single integrated circuit. Because, according to the specification, prior art memory devices could perform only one memory operation at a time, data processing systems were forced to wait for the peripheral memory device to complete each memory operation before beginning to process a subsequent instruction. As a result, the overall performance of a data processing system was often limited by the operating frequency of the peripheral memory device-regardless of the operating frequency of the other components of a data processing system. '494 patent, 1 :14-23. The '494 patent purports to provide a cost-effective solution to this performance bottleneck by allowing for concurrent memory accesses in a single integrated circuit.

2. Agreed Constructions

The parties do not agree to the construction of any claim term of the '494 patent.

3. Disputed Constructions

The parties dispute the construction of 11 terms of the '494 patent. As with the '455 patent, the parties agreed to address only five of the disputed terms at the Markman hearing and to rely on the briefing alone for the six remaining disputed terms. The court will construe the terms addressed at the hearing first.

Claim 9 is an independent method claim and is the only independent claim of the '494 patent asserted in this litigation. It provides:

A method for accessing a memory in an integrated circuit, comprising the steps of:

receiving a first instruction for executing a first memory operation, the first instruction indicating a first memory location;

decoding the first instruction to indicate a first one of a plurality of memory banks to be accessed during execution of the first memory operation;

storing a first address value in a first latch circuit in the first one of the plurality of memory banks, the first address value corresponding to a first memory location in the first one of the plurality of memory banks;

storing a first control value in a second latch circuit in the first one of the plurality of memory banks, the first control value indicating a type of memory operation to be executed, the type of memory operation being one of a read memory operation and a write memory operation;

receiving a second instruction for executing a second memory operation, the second instruction indicating a second memory location to be accessed;

decoding the second instruction to indicate a second one of the plurality of memory banks to be accessed during execution of the second memory operation;

storing a second address value in a first latch circuit in the second one of the plurality of memory banks, the second address value corresponding to a second memory location in the second one of the plurality of memory banks;

storing a second control value in a second latch circuit in the second one of the plurality of memory banks, the second control information value indicating the type of memory operation to be executed; and

concurrently executing the first memory operation in the first one of the plurality of memory banks and the second memory operation in the second one of the plurality of memory banks.

a. An Integrated Circuit (Claims 9, 10, 11)

[23] Freescale argues that "an integrated circuit" is a limitation of claim 9 of the '494 patent and that it means "a single integrated circuit." ProMOS argues that the preamble of claim 9 is not a limitation or, alternatively, that "an integrated circuit" means "at least one integrated circuit." The parties' disputes regarding this term, therefore, are (1) whether the preamble is a limitation of claim 9 and (2) whether, if the preamble is a limitation, "an" means "one" or "one or more." FN5 The preamble of claim 9 states: "A method for accessing a memory in an integrated circuit, comprising the steps of."

FN5. The parties agreed at the Markman hearing that the term "integrated circuit" need not be construed.

[24] [25] [26] In general, "a claim preamble has the import that the claim as a whole suggests for it." Bell Commc'ns Res., Inc. v. Vitalink Comm'ns Corp., 55 F.3d 615, 620 (Fed.Cir.1995). "In other words, when the claim drafter chooses to use *both* the preamble and the body to define the subject matter of the claimed invention, the invention so defined, and not some other, is the one the patent protects." Id. In somewhat more specific terms, "a preamble limits the invention if it recites essential structure or steps, or if it is 'necessary to give life, meaning, and vitality' to the claim." Catalina Marketing Int'l, Inc. v. Coolsavings.com, Inc., 289 F.3d 801, 808 (Fed.Cir.2002) (quoting Pitney Bowes, Inc. v. Hewlett-Packard Co., 182 F.3d 1298, 1305 (Fed.Cir.1999)). A preamble is not limiting, however, "where a patentee defines a structurally complete invention in the claim body and uses the preamble only to state a purpose or intended

use for the invention." Rowe v. Dror, 112 F.3d 473, 478 (Fed.Cir.1997).

[27] Moreover, "clear reliance on the preamble during prosecution to distinguish the claimed invention from the prior art transforms the preamble into a claim limitation because such reliance indicates use of the preamble to define, in part, the claimed invention." Catalina Marketing, 289 F.3d at 808-09.

In claim 9 of the '494 patent, the preamble describes the specific structure in which the claimed method is performed. "An integrated circuit" is thus necessary to give life, meaning, and vitality to the claim. The "Summary of the Invention" likewise states that "[t]he storage banks are implemented in a single integrated circuit," revealing that the patentee intended for the invention to be performed within a single integrated circuit, and not in some other structure or within multiple integrated circuits. '494 patent, 3 :5-6. Moreover, the patentee distinguished prior art during prosecution on the basis that a prior art patent "is not implemented on a single integrated circuit" but that "[t]he claimed invention ... is implemented on an integrated circuit." Plaintiff's Ex. 12 at 11, 16. The patentee thus relied on the preamble to define, in part, the claimed invention, and the preamble of claim 9 is a claim limitation.

[28] Federal Circuit precedent establishes that "a" or "an" ordinarily means "one or more." *See* Tate Access Floors, Inc. v. Interface Arch. Res., Inc., 279 F.3d 1357, 1370 (Fed.Cir.2002); Collegenet, Inc. v. Applyyourself, Inc., 418 F.3d 1225, 1232 (Fed.Cir.2005). However, the ordinary and customary meaning of a term is not always the proper interpretation of a claim term. Phillips instructs the court to analyze the claim term not only in the context of the particular claim in which the disputed term appears, but in the context of the entire intrinsic record. 415 F.3d at 1313.

As described above, the patentees described that "[t]he storage banks are implemented in a single integrated circuit" in the "Summary of the Invention" section of the specification. '494 patent, 3 :5-6. And tellingly, the patentees distinguished several prior art references during prosecution based in part on the fact that the prior art was "not implemented in a single integrated circuit," but that this invention "is implemented on an integrated circuit." Plaintiff's Ex. 12 at 10-12; *see* Plaintiff's Ex. 22 at 5. Because the patentees summarized this invention as being implemented in a single integrated circuit and distinguished prior art on this basis during prosecution, "an integrated circuit" means "a single integrated circuit." FN6

FN6. ProMOS also argues that claim 9 must necessarily be performed in more than one integrated circuit, although it provides no evidence to support this argument. And even its own proposed construction encompasses a single integrated circuit. If claim 9 required more than a single integrated circuit to be performed, the court would expect the proposed construction to be "at least two integrated circuits" or the like.

b. Memory Operation (Claims 9, 10, 11)

[29] Freescale argues that this term means "cycle of actions performed to retrieve, store, or refresh data in a memory bank." ProMOS argues that this term means "a process of accessing a memory location and performing a read or write action." The dispute again centers on two issues: (1) whether a "refresh" memory operation should be explicitly included in the construction and (2) whether a memory operation includes the entire cycle of actions performed to read or write (or refresh) data.

The '494 patent describes that memory element 46 in a preferred embodiment may be a DRAM. '494 patent,

14:7-11. At the Markman hearing, the parties agreed that a "refresh" memory operation is performed within a DRAM (dynamic random access memory) device, which the parties agreed is neither a read operation nor a write operation. The specification thus allows for the possibility that a "refresh" memory operation is performed in memory element 46 in a preferred embodiment of the invention. The issue for the court is whether the term "memory operation" in claims 9-11 encompasses the "refresh" memory operation contemplated in this preferred embodiment.

Claim 9 of the '494 patent references a first memory operation and a second memory operation. The type of the first memory operation is "one of a read memory operation and a write memory operation." '494 patent, 16 :7-11. The second memory operation, unlike the first memory operation, is *not* limited to a read or write memory operation by subsequent claim language. *Id*. at 16:24-28. The second memory operation, therefore, may be a read memory operation, write memory operation, or another type of memory operation (such as a refresh operation). If, as ProMOS argues, the term "memory operation" was limited to read and write operations, the claim language qualifying the type of first memory operation in claim 9 would be superfluous. Such a construction would also vitiate the claim's distinction between the first memory operation (which is limited to a read or write operation) and the second memory operation (which is not so limited). The broader term "memory operation" (which includes both the first and second memory operations), therefore, includes a refresh memory operation.

The remaining dispute is whether "memory operation" should encompass only a portion of the steps performed in an integrated circuit during a memory operation or whether it encompasses the entire cycle of actions performed during a memory operation. In other words, the parties disagree over which steps are included in "Reading A," "Writing B," and "Reading C" in Figure 4 of the '494 patent. As described in the specification, successive memory operations in the prior art could not begin until the previous memory operation was complete. The "Background of the Invention" explains that "[t]he time from the start of execution of an operation [such as a read operation] until the device may execute another operation is referred to as the 'cycle time.' " ' 494 patent, 2 :31-33. The cycle time thus spans an entire memory operation.

The "Summary of the Invention" describes that, in the invention, "a plurality of the storage banks [in a single integrated circuit] are accessed during a plurality of multiple overlapping time periods." '494 patent, 3 :5-8. This stands in contrast to the prior art, which the patentee described as unable to overlap successive memory operations in an integrated circuit. *See id*. at 2:46-52. Extrinsic evidence provided by Freescale (Plaintiff Exs. 9A-9D) establishes that the cycle time of a memory operation is comprised of the time required to perform multiple steps, including memory location activation and deactivation steps. The parties agree that activation and deactivation occur in read, write, and refresh memory operations, although they disagree whether those steps are part of a "memory operation" within the meaning of claims 9-11.

ProMOS provides no support for limiting the term "memory operation" to exclude activation and deactivation steps involved in read, write, or refresh memory operations. While ProMOS's proposed construction does not necessarily exclude memory location activation and deactivation steps ("a *process* of accessing ... and performing ..."), the court believes a jury would be best assisted by a construction that explicitly includes all steps performed during a read, write, or refresh memory operation. The term "memory operation," therefore, means "the entire process of accessing a memory location, including activating and deactivating, and performing a read, write, or refresh action in a memory bank."

c. Instruction (Claim 9)

Freescale argues that this term means "a plurality of signals for executing a memory operation." ProMOS argues that this term means "statement that specifies an operation to be performed by a system and that identifies data involved in the operation."

The first method step of claim 9 establishes what an "instruction" specifies: "receiving a first instruction for executing a first memory operation, the first instruction indicating a first memory location." '494 patent, 15 :59-61. It would thus be redundant to include "for executing a memory operation" in this construction.

Subsequent language of claim 9 specifies that a control value (which must necessarily be derived from the instruction) indicates a type of memory operation to be executed, '494 patent, 16 :7-11, so it is likewise unnecessary to include this limitation in the construction of this term. And finally, while an "instruction" indicates a memory location (that is, the location of data involved in the operation), *see id*. 15:59-61, it does not necessarily identify the data involved in the operation.

The term "instruction" is a generic term that simply means "one or more electronic signals." The court ordered the parties on September 27, 2007 to confer and use their best efforts to reduce the number of disputed claim terms in this case. Docket No. 59. The parties were unable to reach agreement on any additional terms, and have left 29 terms to be construed by the court. The court believed, and continues to believe, that the parties should have been able to substantially reduce the number of disputed terms. This term is just one example of a dispute between the parties that absorbed pages of the parties' briefing, the court's and the parties' time at the Markman hearing, and now space in this Claim Construction Order.

d. Concurrently (Claim 9)

[30] Freescale argues that this term means "overlapping any of the actions in a first memory operation with any of the actions in a second memory operation." ProMOS argues that this term means "operating or occurring at the same time." ProMOS also argues that its proposed construction does not require absolute simultaneity, but that it would require "meaningful" or "substantial" overlap of the memory operations.FN7 The central dispute, therefore, is whether the construction of this term should include a limitation regarding the degree to which memory operations must overlap to be considered "concurrent." The ordinary meaning of "concurrent," according to a dictionary definition cited by ProMOS, is "occurring at the same time." Defendant Ex. 24. However, dictionaries are not the proper place to begin the claim construction analysis under Phillips, and such a definition is not informed by the clear meaning of this term within the context of the ' 494 patent. The ' 494 patent makes clear, in at least three separate places, exactly what the patentee intended the term "concurrently" to mean. First, the parties agree that Figure 4 illustrates three concurrent memory operations, which begin and end at different times. In other words, there is not absolute simultaneity among the three operations, although they there is some degree of overlap. The "Summary of the Invention" section of the specification explains that "the storage banks are implemented in a single integrated circuit and a plurality of the storage banks are accessed during a plurality of multiple overlapping time periods." ' 494 patent, 3:5-8. In other words, the storage banks are accessed concurrently, which is shown graphically in Figure 4. Neither this portion of the specification nor any other portion of the specification describes the degree to which the concurrent memory operations must overlap. Indeed, the patentee's description of the prior art establishes that the prior art did not allow *any* overlap between successive memory operations-unlike the present invention. ' 494 patent, 1:14-3:8.

FN7. While ProMOS's proposed construction would not inform a jury how much overlap is required to be considered "concurrent," the court's analysis will take into account ProMOS's explanation of what it argues

is implicitly required by its proposed construction.

Finally, the "Background of the Invention" section also confirms what the patentee meant by the term "concurrently": "the time necessary to begin execution of subsequent operations is shortened, since the subsequent operations are executed concurrently with the first memory access. Although the cycle time of each of the peripheral memory devices remains the same, the data processing system is able to overlap the accesses of each of the peripheral memory devices and, therefore, increases the number of operations executed in a given amount of time." '494 patent, 2:37-45. While this portion of the specification is addressing the patentee's description of the prior art, it uses the term "concurrently" consistent with its use in describing the invention.

In opposition to Freescale's proposed construction, ProMOS argues that the original claims of the application that ultimately issued as the '494 patent-including a limitation of "time overlapping memory accesses"-were rejected during prosecution as unclear. In response to the examiner's rejection, ProMOS argues, the patentee replaced that term with "concurrently," which added the requirement of "meaningful" or "substantial" overlap between successive memory operations. However, the examiner's rejection was not based on prior art, and the patentee was not forced to narrow the scope of the claims to avoid prior art. Defendant Ex. 16 at 3-4. Instead, the patentee replaced the claim term "time overlapping memory accesses" with the more succinct "concurrently," which, as explained in the specification, has the same meaning. Indeed, the '494 patent is entitled "Randomly Accessible Memory Having Time Overlapping Memory Accesses."

For the foregoing reasons, the term "concurrently" means "overlapping any of the actions in a first memory operation with any of the actions in a second memory operation."

e. Address Value (Claims 9, 10, 11)

[31] Freescale does not believe that this term needs to be construed or, alternatively, that it means "information corresponding to a memory location." ProMOS argues that this term means "a set of numbers that designates an address."

While it does not appear that this term needs to be construed in order to aid a jury's understanding of the claim, the parties insisted at the Markman hearing that the meaning of this term is a point of contention. And while neither party was able to provide the court, at the Markman hearing, with an example of an address value that is *not* a number or set of numbers, the court finds that it is unnecessary to limit the address value to "a set of numbers." From the context of claim 9 and the remainder of the specification, "address value" means "information that designates a memory location."

f. Memory Banks

[32] Freescale argues that "memory banks" are "independently addressable and randomly accessible sections of memory," while ProMOS argues that they are "memory arrays wherein each such array is independently and distinctly addressed and controlled." The parties' dispute is two-fold: (1) whether a memory bank is a "section of memory" or a "memory array," and (2) whether the sections or arrays of memory must be independently and distinctly controlled.

As the "Summary of the Invention" explains:

The randomly accessible memory is comprised of a plurality of storage banks. Each storage bank is independently addressable.... The storage banks are implemented in a single integrated circuit and a plurality of the storage banks are accessed during a plurality of multiple overlapping time periods.

'494 patent, 2:67-68. The specification further explains that, in a preferred embodiment, memory device 28 comprises, among other things, a plurality of memory banks, such as memory bank 34 and memory bank 52 of FIG. 4. '494 patent, 6:13-21.

First, ProMOS correctly argues that Freescale's proposed construction does not differentiate between memory that is organized into memory banks (arrays) and memory that has no such organization. ProMOS Br. at 54. That is, every byte (or other arbitrary subdivision) in a memory would satisfy Frescale's proposed construction ("section of memory"). Because a "memory bank" is a finite subdivision of memory, the court finds that memory banks comprise arrays of memory.

Second, in support of its proposed exclusion of "control" from this construction, Freescale argues that the patentee described memory banks in the prior art as being independently controlled, but explicitly chose not to do so in the "Summary of the Invention." *Compare* '494 patent, 1:67-68 *with* 2:67-68. Freescale is correct in arguing that the "Background of the Invention" describes interleaved memory banks that are independently addressed and controlled, while the "Summary of the Invention" does not mention control. However, this comparison ignores the remainder of the specification.

The title of the '494 patent is "Randomly Accessible Memory Having Time Overlapping Memory Accesses." As the "Summary of the Invention" explains, "[t]he storage banks are implemented in a single integrated circuit and a plurality of the storage banks are accessed during a plurality of multiple overlapping time periods." '494 patent, 3:5-8. In the implementation of preferred embodiment data processing system 22-unlike the known data processing system 10 (FIG.1(A))-time overlapping memory access is accomplished "as a result of the independent control and subsequent overlapped timing of the array of memory banks." Id. at 11:18-30. Indeed, as illustrated in FIG. 4, independent control of memory bank 34, memory bank 52, and memory bank K allows each of the memory banks to be accessed during a plurality of multiple overlapping time periods-without the need for interleaving. The court thus finds that the memory banks of claims 9-11 are independently addressed and controlled.

Moreover, the court finds-as reflected in Freescale's proposed construction-that the claims in which this term appears are limited to randomly accessible memory. Indeed, the "Summary of the Invention" explains that "there is provided, in one form, a randomly accessible memory having time overlapping memory accesses," '494 patent, 2:63-65, and the title of the patent, as mentioned above, is "Randomly Accessible Memory Having Time Overlapping Memory Accesses."

Accordingly, the court construes this term to mean "randomly accessible memory arrays wherein each such array is independently addressed and controlled."

g. Memory Location

[33] Freescale argues that this term does not need to be construed or, alternatively, that it means "an addressable portion of a memory bank where data can be stored and retrieved." ProMOS argues that "memory location" means "unit of storage space in the memory that is uniquely specified by means of an

address." The parties' dispute, therefore, is whether "memory location" is an unidentified "unit" of storage space or a portion of a memory bank that is "addressable."

The parties' arguments in support of their proposed constructions reveal that their constructions do not substantively differ. ProMOS's primary criticism of Freescale's proposed construction is that it encompasses any quantity of memory, from a bit to an entire memory bank. ProMOS Br. at 65. ProMOS, however, does not identify to what "unit of storage space" its construction refers. Indeed, as Freescale correctly argues, an undefined "unit of storage space" could likewise encompass any size unit of memory-from a bit to an entire memory bank. Because ProMOS's proposed construction would not clarify to a juror the specific "unit" of storage space that qualifies as a memory location, the court finds that this construction should instead refer to an addressable portion of a memory bank.

The court thus construes "memory location" to mean "an addressable portion of a memory bank where data can be stored and retrieved."

h. Control Value, Control Information, and Control Information ValueFN8

FN8. The parties agree that these three terms should be construed to have the same meaning.

[34] Freescale argues that these terms do not need to be construed or, alternatively, that they mean "information indicating a type of memory operation to be executed." ProMOS argues that these terms mean "number set by a control signal."

ProMOS's proposed construction limits these terms to a "number," while Freescale's proposed construction includes any information indicating a type of memory operation to be executed. The '494 patent uses these terms throughout the patent, consistently referring to control information necessary to perform a memory accessoperation. *See, e.g.,* '494 patent, 5:11-13, 35-39, 42-45. Because the patent does not limit the meaning of these terms to one "number"-indeed, a "control value" could rather be a set of numbers-the court construes this term to mean "information indicating a type of memory operation to be executed."

i. External Data Output Control Value

[35] Freescale argues that this term does not need to be construed or, alternatively, that it means "information corresponding to a signal that determines when to enable or disable the data output driver." ProMOS argues that it means "number corresponding to an externally supplied signal that (i) indicates the address of the memory location that stores the data to be output and (ii) indicates timing for outputting data."

The specification describes that, in a preferred embodiment, a "Data Out Strobe" (i.e., a control signal) is used to enable the data output driver of Memory Device 28 to output an information value to Data Processor 24 via the Data Out signal. *See, e.g.,* '494 patent, 5:50-55, 7:40-45, 9:28-35. The Data Out Strobe is thus an example of an "external data output control value"-i.e., it is information corresponding to a signal that determines when to enable or disable the data output driver of the memory device.

ProMOS argues that the external data output control value must also indicate the address of the memory location that stores the data to be output and indicate timing for outputting data, but fails to identify support in the specification for such a construction incorporating these additional limitations.

Accordingly, the court construes this term to mean "information corresponding to a signal that determines when to enable or disable the data output driver."

V. THE '816 PATENT

1. Background of the Technology

In general, the '816 patent describes a process for forming a semiconductor device that increases device reliability. During manufacturing of a semiconductor device, metal-containing layers are applied over insulating layers, after which portions of the metal-containing layers are etched away (that is, chemically removed). The process of applying metal-containing layers and selectively etching portions of those layers eventually forms communication pathways within a semiconductor device. During the manufacturing process, however, mobile ions are introduced, which degrade device reliability by interfering with a device's electrical connections. The '816 patent purports to identify a previously unknown location of mobile ions and discloses a process for removing a substantial majority of those ions during the manufacturing process.

The '816 patent describes how mobile ions are deposited both on and within the insulating layer during the semiconductor manufacturing process. Conventional wisdom prior to the invention, explains the patentee, was that mobile ions introduced during the manufacturing process lie only on exposed surfaces. '816 patent, 1:20-24. The prior art, therefore, consisted of deionized water rinses, which removed "virtually all of the mobile ions" on the exposed surfaces during manufacturing. '816 patent, 1:24-26. But even after the deionized water rinses, semiconductor devices suffered reliability problems. The '816 patent describes the cause of the continued unreliability as mobile ions implanted into the insulating layer but not removed with a deionized water rinse. '816 patent, 1:26-28.

The '816 patent discloses an additional etching step, in which a fluoride-containing solution etches the upper portion of the insulating layer, designed to remove a substantial majority of the implanted mobile ions.

2. Agreed Constructions

The parties do not agree to the construction of any terms of the '816 patent.

3. Disputed Constructions

The parties dispute the construction of four terms of the '816 patent, although they agree that two of the four terms should be construed to have the same meaning.

Claim 9 is an independent process claim and is representative of how the disputed claims terms are used in the asserted claims. It provides:

A process for forming a semiconductor device comprising the steps of:

forming a first insulating layer over a semiconductor substrate;

depositing a metal-containing layer over the first insulating layer;

forming a patterned organic masking layer over the metal-containing layer thereby forming exposed portions

of the metal-containing layer;

etching the exposed portions of the metal-containing layer with a halide-containing plasma etchant to form an interconnect member;

removing the patterned organic masking layer with a plasma gas;

etching a portion of the first insulating layer with a fluoride-containing solution, wherein this step:

removes at least 75 percent of mobile ions from the first insulating layer; and is performed after the step of etching the exposed portions and prior to forming any layer over the interconnect member; and

forming a second insulating layer over the interconnect member.

a. Metal-containing layer (Claims 1, 6, 9, 13)

[36] Freescale argues that this term means "layer of material whose thickness includes at least metal," while ProMOS argues that it means "a layer that contains a sufficient quantity of metallic elements such that it can serve as a conductive layer."

The '816 patent refers to insulating layers and interconnecting layers deposited and etched during the semiconductor device manufacturing process. *See, e.g.,* '816 patent, 3:42-49. As explained in the specification, "[t]he interconnecting layer 41 is a metal-containing layer...." Id. 4:13-14. The ' 816 patent thus uses the terms "metal-containing layer" and "interconnecting layer" synonymously and distinguishes both from the insulating layer. ProMOS argues, correctly, that under Freescale's proposed construction, even insulating layers would be considered "metal-containing layers" because, according to the patent, metal ions are implanted within the insulating layer during the manufacturing process. Under Freescale's proposed construction, then, even an insulating layer's thickness would include at least metal.

Freescale argues that ProMOS's proposed construction improperly requires that the metal-containing layer be conductive at the time it is deposited. As Freescale argued at the Markman hearing, it may be possible for additional manufacturing steps to occur between the step of depositing the metal-containing layer and the step of etching the exposed portions of the metal-containing layer. Those additional steps may, for example, render conductive a previously non-conductive layer, or render a metal-containing layer capable of forming an interconnect member. Such a process, Freescale argues, would still fall within the proper scope of the "comprising" claim yet would be improperly excluded under ProMOS's proposed construction. *See* Genentech, Inc. v. Chiron Corp., 112 F.3d 495, 501 (Fed.Cir.1997) (" 'Comprising' is a term of art used in claim language which means that the named elements are essential, but other elements may be added and still form a construct within the scope of the claim.").

The court notes that neither the word "conduct" nor the word "conductive" appears in the '816 patent and, therefore, declines to introduce the term in this construction. The metal-containing layer need only be capable of forming an interconnect member at the time it is etched; the intrinsic record does not require that the metal-containing layer necessarily be conductive or be capable of forming an interconnect member at the time it is deposited. It also does not prohibit additional manufacturing steps not specifically recited in the claim. Regardless of whether such steps are possible or desirable, the intrinsic record does not support excluding such a possibility from the scope of these claims. As used in the claims of the ' 816 patent,

"metal-containing layer" means "layer that, when etched, is capable of forming an interconnect member." FN9

FN9. Freescale agreed with this construction at the Markman hearing.

b. Mobile Ions (Claims 2, 9)

[37] Freescale argues that this term means "Group IA and IIA metal ions introduced during the metal etch processing sequence," while ProMOS argues that it means "sodium, lithium, potassium, calcium and magnesium ions that are located anywhere within (and are not on top of or on the surface of) the first insulating layer." The parties agree that "mobile ions" are metal ions that degrade device reliability and that are capable of moving through at least the insulating layer during the manufacturing process. *See* Plaintiff's Br. at 28; Defendant's Br. at 35; '816 patent, 1:13-29. The parties' dispute boils down to which metal ions should be included in this construction and where those metal ions must be located in the semiconductor device.

The court first notes that the intrinsic record does not refer to mobile ions as being metal ions from Group IA and IIA of the periodic table. In response to Freescale's proposal that the term "mobile ions" includes *all* Group IA and IIA metal ions, ProMOS submitted a journal article suggesting that, at least under some conditions, certain Group IA and IIA metal ions are not mobile. *See* Defendant Ex. 13. According to ProMOS's unrebutted extrinsic evidence, the large ionic radii of some of those metal ions would prevent them from moving between the atoms of the insulating layer under some conditions. *See* id. Given this extrinsic evidence and the fact that the intrinsic record does not define mobile ions to include all metal ions in Groups IA and IIA of the periodic table, the court finds that Freescale's proposed construction is potentially over-inclusive.

The '816 specification states that "[m]obile ions, such as sodium, lithium, potassium, calcium, and magnesium, typically come from two sources[.]" By using the introductory phrase "such as," the patentee explicitly did not limit mobile ions only to these examples provided in the specification, as suggested by ProMOS. The court thus finds that ProMOS's proposed construction is potentially under-inclusive.

Whether types of metal ions in addition to those specifically listed in the specification should be considered mobile ions will be a question of fact based on the proper construction of this term. The court need not determine this fact question during the claim construction process.

The next issue for the court is whether this term, as used in the claims, includes mobile ions anywhere in the device at any stage of the manufacturing process or only those mobile ions introduced at a certain stage of the process. The specification makes clear that this invention is directed at removing mobile ions introduced during the metal etch processing sequence, which includes, for example, the steps of etching the metal-containing layer and the step of removing an organic masking layer. '816 patent, 1:16-20. The specification goes on to explain that "[t]he conventional wisdom of those skilled in the art is that mobile ions *introduced during the metal etching steps* lie only on exposed surfaces of an insulating layer or an interconnect formed during the metal etching process." Id. at 1:20-24 (emphasis added). Later in the specification, the patentee explained that "[e]mbodiments of the present invention may be used to reduce mobile ion contamination that is introduced into a semiconductor device around the point in processing during steps of a metal etch processing sequence or a resist-etch-back processing step." '816 patent, 3:21-25. The specification

additionally explains that "[b]y eliminating the organic masking layer solvent and etching some of the insulating layer after the plasma metal etching step, mobile ion contamination *introduced during the metal etch processing sequence* may be substantially reduced." '816 patent, 3:28-32 (emphasis added). Moreover, the patentee distinguished prior art based on the fact that-unlike the invention-the prior art "does not teach or suggest that mobile ions are being implanted into the wafer *during the etch step*." Plaintiff Ex. 12 (emphasis added). The intrinsic record thus makes clear that the mobile ions at which the invention is directed are those that are introduced during the etch processing sequence of the metal-containing layer.

Because the generic term "mobile ions" does not distinguish between those mobile ions that are introduced *on* the insulating layer and those introduced *into* the insulating layer during the etch processing sequence of the metal-containing layer, the court finds that the parties' dispute concerning this limitation is more appropriately addressed in the construction of the entire claim phrase below. The term "mobile ions" means "metal ions that degrade device reliability, are capable of moving through the insulating layer during the manufacturing process, and are introduced on or into the insulating layer during the etch processing sequence of the metal-containing layer."

c. "Etches at least 75 percent of mobile ions from the first insulating layer" (Claim 2) or "removes at least 75 percent of mobile ions from the first insulating layer" (Claim 9)FN10

FN10. The parties agreed during briefing that these two phrases have the same meaning.

[38] Freescale argues that this term does not need to be construed or, alternatively, that it means "reduces the concentration of mobile ions from the first insulating layer by at least 75 percent." ProMOS argues that this term means "removing at least 75 percent of the combined total of all sodium, lithium, potassium, calcium and magnesium ions that are located anywhere within (and are not on top of or on the surface of) the first insulating layer, where secondary ion mass spectrometry ("SIMS") is used to determine whether the 75 percent limitation is satisfied." FN11 The parties' dispute centers on how to calculate whether the 75 percent limitation has been satisfied. That is, what is the total number of mobile ions, 75 percent of which must be removed? The sole remaining dispute regarding this construction, given the court's construction of the term "mobile ions," above, is whether the total number of mobile ions for purposes of the 75 percent calculation are only those mobile ions located within the insulating layer, or whether it includes both those mobile ions located within the insulating layer and those mobile ions located on top of the insulating layer. This construction, therefore, is a construction of the word "from" as used in this phrase: "remov[ing] at least 75 percent of mobile ions *from* the first insulating layer." ' 816 patent, 12:48-49.

FN11. The court notes that the parties agreed at the Markman hearing that SIMS or equivalents may be used to determine whether this limitation is satisfied. *See* '816 patent, 10:7-10. The method of measurement, however, is unnecessary to specify in the construction of this phrase, and the court declines to do so. Whether a method of measurement is equivalent to SIMS will be a fact question determined at trial.

The claims themselves provide some insight into the meaning of this phrase. Independent claim 9 contains the limitation that the "etching a portion of the first insulating layer" step "removes at least 75 percent of mobile ions from the first insulating layer." '816 patent, 12:48-49. Dependent claim 13 (dependent on claim 9) adds a further step of "rinsing the substrate with deionized water between the steps of etching the exposed portions of the metal-containing layer and etching the portion of the first insulating layer." '816

patent, 13:2-4. As explained in the specification, a deionized water rinse after the etching of the metal-containing layer (and prior to the etching of the first insulating layer) "should remove virtually all of the mobile ions if they lie on exposed surfaces." '816 patent, 1:24-26. Under Freescale's proposed construction, then, claim 13 is likely impossible to infringe because virtually all of the mobile ions on exposed surfaces are removed by the deionized water rinse step. Therefore, fewer than 75% of mobile ions remain at the time the "etching the portion of the first insulating layer" step is performed. While not dispositive, the claims support ProMOS's proposed construction.

The specification discusses removing 75 percent of the mobile ions six times other than in the claims. Three of those instances track the disputed claim language: removing 75 percent of the mobile ions *from* the insulating layer. *See* '816 patent, 2:15-18; 2:32-35; and 9:36-43. Only one of these instances provides insight to the meaning of this claim term. In the "Benefits" section of the specification, the patent states that "[m]obile ions that are *implanted into* the insulating layer from the plasma metal etching step may be virtually eliminated from the plasma metal etching step by etching the surface of the insulating layer using an etching solution. The etching removes at least 75 percent of the mobile ions *from* the insulating layers and should remove at least 95 percent of all mobile ions from the insulating layers." ' 816 patent, 9:36-43 (emphasis added). In this portion of the specification, then, the patentee uses the phrase " *from* the insulating layers" to refer to the mobile ions " *implanted into* the insulating layer" and indicates that the implanted mobile ions may be "virtually eliminated" by the invention's removal of at least 75-95 percent.

The other three instances in the specification discussing the removal of 75 percent of the mobile ions are consistent with the above. First, the Abstract explains that "[t]he etch removes at least 75 percent of the mobile ions *within* the insulating layer" (emphasis added). In the "Benefits" section of the specification, the patentee twice states that the removal "of oxide thicknesses less than 100 angstroms may result in less than a 75 percent reduction of mobile ions *in* the insulating layer." '816 patent, 10:24-26; 10:41-43.

The specification thus uses the terms "in," "within," and "from" interchangeably. While the patentee chose to use three different words in describing the 75 percent mobile ion reduction in the specification, the most reasonable reading of the claims and specification is that the patentee intended to consistently describe what was being removed: "virtually all" of the newly discovered implanted mobile ions. If, as Freescale's proposed construction would implicitly allow, the total number of mobile ions for purposes of the 75 percent calculation included both those within and those on the surface of the insulating layer, even the prior art deionized water rinse would remove 75 percent of the mobile ions.FN12 In the context of the claims and the specification, therefore, this term means "removing, by etching, at least 75 percent of mobile ions that are within (and not on the surface of) the first insulating layer."

FN12. Though Freescale's proposed construction does not explicitly describe whether it includes the mobile ions implanted into the insulating layer and/or those on the surface of the insulating layer, it will be most helpful to a jury to explain the universe of mobile ions for purposes of the 75 percent calculation.

CONCLUSION

Based on the foregoing, the court construes the disputed terms and limitations of the '455, '494 and '816 patents as set forth above.

IT IS SO ORDERED.

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