United States District Court,
E.D. Texas, Marshall Division.

MICRON TECHNOLOGY, INC. and Micron Semiconductor Products, Inc,
Plaintiffs.
v.
TESSERA, INC,
Defendant.

Civil Action No. 2:05cv319

July 13, 2006.

Background: Patentee brought action against alleged infringer for infringement of patents for microchip packaging. Parties requested construction of claims.

Holdings: The District Court, Love, United States Magistrate Judge, held that:
(1) claims were not written in Jepson format;
(2) preambles were limiting; and
(3) "conductive leads" meant conductive input/output (I/O) elements on the outside of a self-contained die package.

So ordered.

36,325. Construed.

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MEMORANDUM OPINION AND ORDER

LOVE, United States Magistrate Judge.

This claim construction opinion construes terms in U.S. Patent Nos. 4,992,849 ("the '849 patent"), 5,107,328 ("the '328 patent"), and Re. 36,325 ("the '325 patent"). Plaintiffs, Micron Technology, Inc. and Micron Semiconductor Products, Inc. (collectively "Micron"), have asserted several other patents against Defendant, Tessera, Inc. ("Tessera"), in this lawsuit, but only claim language from the '849, '325, and '328 patents remains in dispute.

The Patents

The patents in suit generally deal with microchip packaging. The '328 patent describes a means for packaging a semiconductor die with centrally or laterally locatedbond pads without the use of a lead frame. In the past, as semiconductor dies got smaller, new smaller frames also had to be designed. By dispensing with the lead frame altogether, the '328 patent allows the package to accommodate smaller dies without the necessity of designing another lead frame. The package houses the die in a series of shelves, which are capped by a lid and a base.

Both the '849 and '325 patents relate to means for connecting multiple semiconductor die onto a polymide substrate where the substrate functions as both a lead frame connection for the semiconductor die and as a printed circuit board.

Applicable Law

[1] [2] [3] "It is a 'bedrock principle' of patent law that 'the claims of a patent define the invention to which the patentee is entitled the right to exclude." Phillips v. AWH Corp., 415 F.3d 1303, 1312 (Fed.Cir.2005) (en banc) (quoting Innova/Pure Water Inc. v. Safari Water Filtration Sys., Inc., 381 F.3d 1111, 1115 (Fed.Cir.2004)). In claim construction, courts examine the patent's intrinsic evidence to define the patented invention's scope. *See id.;* C.R. Bard, Inc. v. U.S. Surgical Corp., 388 F.3d 858, 861 (Fed.Cir.2004); Bell Atl. Network Servs., Inc. v. Covad Communications Group, Inc., 262 F.3d 1258, 1267 (Fed.Cir.2001). This intrinsic evidence includes the claims themselves, the specification, and the prosecution history. *See* Phillips, 415 F.3d at 1314; C.R. Bard, Inc., 388 F.3d at 861. Courts give claim terms their ordinary and accustomed meaning as understood by one of ordinary skill in the art at the time of the invention in the context of the entire patent. Phillips, 415 F.3d at 1312-13; Alloc, Inc. v. Int'l Trade Comm'n, 342 F.3d 1361, 1368 (Fed.Cir.2003).

[4] [5] [6] The claims themselves provide substantial guidance in determining the meaning of particular claim terms. Phillips, 415 F.3d at 1314. First, a term's context in the asserted claim can be very instructive. *Id*. Other asserted or unasserted claims can also aid in determining the claim's meaning because claim terms are typically used consistently throughout the patent. *Id*. Differences among the claim terms can also assist in understanding a term's meaning. *Id*. For example, when a dependent claim adds a limitation to an independent claim, it is presumed that the independent claim does not include the limitation. *Id*. at 1314-15.

[7] [8] [9] [10] Claims "must be read in view of the specification, of which they are a part." *Id*. (quoting Markman v. Westview Instruments, Inc., 52 F.3d 967, 978 (Fed.Cir.1995)). "[T]he specification 'is always highly relevant to the claim construction analysis. Usually, it is dispositive; it is the single best guide to the meaning of a disputed term.' " *Id*. (quoting Vitronics Corp. v. Conceptronic, Inc., 90 F.3d 1576, 1582 (Fed.Cir.1996)); Teleflex, Inc. v. Ficosa N. Am. Corp., 299 F.3d 1313, 1325 (Fed.Cir.2002). This is true because a patentee may define his own terms, give a claim term a different meaning than the term would otherwise possess, or disclaim or disavow the claim scope. Phillips, 415 F.3d at 1316. In these situations, the inventor's lexicography governs. *Id*. Also, the specification may resolve ambiguous claim terms "where the ordinary and accustomed meaning of the words used in the claims lack sufficient clarity to permit the scope of the claim to be ascertained from the words alone." Teleflex, Inc., 299 F.3d at 1325. But, "although the specification may aid the court in interpreting the meaning of disputed claim language, particular

embodiments and examples appearing in the specification will not generally be read into the claims." Comark Communications, Inc. v. Harris Corp., 156 F.3d 1182, 1187 (Fed.Cir.1998); *see also* Phillips, 415 F.3d at 1323. The prosecution history is another tool to supply the proper context for claim construction because a patent applicant may also define a term in prosecuting the patent. Home Diagnostics, Inc., v. LifeScan, Inc., 381 F.3d 1352, 1356 (Fed.Cir.2004) ("As in the case of the specification, a patent applicant may define a term in prosecuting a patent.").

[11] [12] [13] [14] Although extrinsic evidence can be useful, it is "less significant than the intrinsic record in determining 'the legally operative meaning of claim language.' " Phillips, 415 F.3d at 1317 (quoting C.R. Bard, Inc., 388 F.3d at 862). Technical dictionaries and treatises may help a court understand the underlying technology and the manner in which one skilled in the art might use claim terms, but technical dictionaries and treatises may provide definitions that are too broad or may not be indicative of how the term is used in the patent. *Id*. at 1318. Similarly, expert testimony may aid a court in understanding the underlying technology and determining the particular meaning of a term in the pertinent field, but an expert's conclusory, unsupported assertions as to a term's definition is entirely unhelpful to a court. *Id*. Generally, extrinsic evidence is "less reliable than the patent and its prosecution history in determining how to read claim terms." *Id*.

The Terms

The '849 and '325 Patents

Proceeding on two separate theories, Tessera argues that the preambles to Claim 1 of the '849 and '325 patents limit those claims. FN1 Tessera's first theory is that these claims were written in Jepson form because they "first describe the scope of the prior art and then claim an improvement of the prior art." Dow Chem. Co. v. Sumitomo Chem. Co., Ltd., 257 F.3d 1364 (Fed.Cir.2001); 37 C.F.R. s. 1.75(e). Alternatively, Tessera argues that the preambles are limiting because they recite essential structure that is important to the invention or necessary to give meaning to the claim. NTP, Inc. v. Research In Motion, Ltd., 418 F.3d 1282, 1305-06 (Fed.Cir.2005), *cert. denied,* 546 U.S. 1157, 126 S.Ct. 1174, 163 L.Ed.2d 1141 (2006). The Court finds that both preambles are limiting, but were not written in Jepson form.

FN1. '325 Patent, Preamble to Claim 1: A memory array in which a plurality of memory circuit devices are arranged in a manner such that memory information is obtained by addressing bits of information from a selected number of the memory devices in the array in a format, and the format of bits forms a byte of memory data such that each byte includes bits from each memory device in the selected number of the circuit devices, and wherein the bits are addressed as rows and columns of information in a matrix on each memory device, characterized by.

'849 Patent, Preamble to Claim 1: Board level integrated circuit in which a plurality of semiconductor circuit devices are arranged on a flexible circuit board and each of the semiconductor circuit devices is a distinct integrated circuit chip, characterized by.
[15] 37 C.F.R. s. 1.75(e) sets forth the requirements for Jepson claims, and provides:

Where the nature of the case admits, as in the case of an improvement, any independent claim should contain in the following order: (1) a preamble comprising a general description of all the elements or steps of the claimed combination which are conventional or known, (2) a phrase such as "wherein the improvement comprises," and (3) those elements, steps and/or relationships which constitute that portion of the claimed combination which the applicant considers as the new or improved portion.

Courts rely on Rule s. 1.75(e)(1) when analyzing Jepson issues. *See* Epcon Gas Systems, Inc. v. Bauer Compressors, Inc., 279 F.3d 1022, 1029 (Fed.Cir.2002); Kegel Co. v. AMF Bowling, Inc., 127 F.3d 1420,

1426 (Fed.Cir.1997). In a Jepson claim, the "preamble defines not only the context of the claimed invention, but also its scope." Rowe v. Dror, 112 F.3d 473, 479 (Fed.Cir.1997). By employing the Jepson form the patentee evidences the intention "to use the preamble to define, in part, the structural elements of his claimed invention." Epcon Gas, 279 F.3d at 1029; Rowe, 112 F.3d at 479; Kegel, 127 F.3d at 1426.

[16] Rule s. 1.75(e) and the associated case law require that Jepson claims contain specific information in a narrowly defined form, and the Court is aware of no exceptions to these requirements. In arguing that Claim 1 of the '325 and '849 patents are Jepson claims, Tessera seeks to impermissibly relax these requirements.

Tessera argues that the preambles were drafted in Jepson form because the preamble language corresponds with prior art depicted in Figure 2 of the patent, and because the prior art references in the preamble are further described in the specification. However, the preamble of a Jepson claim must do more than refer to prior art that is more fully described elsewhere in the patent. Rule s. 1.75(e)(1) requires that the preamble set forth a "general description all of the elements or steps of the claimed combination which are conventional or known." Tessera seems to suggest that a preamble written in Jepson form need only refer to prior art to satisfy Rule s. 1.75(e)(1). The Court disagrees.

[17] The preamble of a Jepson claim is drafted to "define, in part, the structural elements of [the] claimed invention." Epcon Gas, 279 F.3d at 1029; Rowe, 112 F.3d at 479; Kegel, 127 F.3d at 1426. Therefore, it is reasonable to require that the preamble set forth the elements or steps of the prior art that are improved upon so that the public may be fairly notified of the scope of the invention. Tessera cites no authority to support its argument that a preamble may be written in Jepson form if what is described in the preamble is described elsewhere in the specification as prior art, and the Court sees no reason to so interpret Rule s. 1.75(e)(1). However, even assuming the preambles of the '849 and '325 comported with Jepson form, these claims lack the necessary transitional phrase indicating that the subsequent language comprises an improvement over the previously stated prior art.

[18] [19] The preambles at issue conclude with the phrase "characterized by," but Rule s. 1.75(e)(2) requires that Jepson claims employ "a phrase *such as* 'wherein the improvement comprises' (emphasis added)." Although the phrase "such as" offers some leeway to the patentee, Tessera cites no authority to suggest the phrase "characterized by" satisfies Rule s. 1.75(e)(2). The caselaw reflects some variation in the phrases used in Jepson claims, but they all communicate that the subsequent claim language constitutes an improvement. Neutrik AG v. Switchcraft, Inc., 31 Fed.Appx. 718, 720 ("the improvement comprising"); Epcon Gas, 279 F.3d at 1029, 1030 ("the improvement wherein"); Dow Chemical v. Sumitomo Chemical Co., Ltd., 257 F.3d 1364 ("the improvement which comprises"); DeMarini Sports, Inc. v. Worth, Inc., 239 F.3d 1314, 1318 ("an improvement comprising"); Kegel, 127 F.3d at 1426, 1423 ("the improvement comprising") Rowe, 112 F.3d at 476 ("the improvement comprising"). All of these phrases communicate that the preceding language described prior art FN2 and the subsequent language describes an improvement over that prior art. The phrase "characterized by" without more, is insufficient to satisfy Rule s. 1.75(e)(2) because it fails to communicate that the subsequent language comprises an improvement over the previously stated elements or steps of prior art. As stated above, the narrowly defined Jepson form must be followed closely so that the public may be notified of the scope of the invention. Therefore, the Court cannot find that Claim 1 of either the '849 or the '325 patents is written in Jepson form.FN3

FN2. The Court is not precluding the possibility that the foregoing language, which would presumably be the preamble, may contain other language not comprising prior art. However, in order to satisfy Rule s. 1.75(e)(2), no prior art may appear after the phrase.

FN3. The Court also notes that Tessera cites no evidence from the prosecution history to suggest that Micron intended to draft these claims in Jepson form. *See* Epcon Gas, 279 F.3d at 1029; Rowe, 112 F.3d at 479;

Kegel, 127 F.3d at 1426. Although other evidence could establish whether Micron intended to draft these claims in Jepson form, the prosecution history can be particularly helpful in determining the patentee's intent. *See* Epcon Gas, 279 F.3d at 1029; Polaroid Corp. v. Eastman Kodak Co., 519 F.Supp. 381, 384 (D.C.Mass.1981).

[20] [21] [22] [23] The Court will now address whether the preambles are limiting without regard to Jepson form. When limitations in the body of a patent claim rely upon, and derive antecedent basis from, the claim preamble, the preamble may act as a necessary component of the claimed invention. Bicon, Inc. v. Straumann Co., 441 F.3d 945, 952 (Fed.Cir.2006). In order to be limiting, the preamble must recite essential structure that is important to the invention or necessary to give meaning to the claim. *Id. citing* NTP, Inc. v. Research In Motion, Ltd., 418 F.3d 1282, 1305-06 (Fed.Cir.2005), cert. denied, 546 U.S. 1157, 126 S.Ct. 1174, 163 L.Ed.2d 1141 (2006). However, a preamble is not considered limiting "where a patentee defines a structurally complete invention in the claim body and uses the preamble only to state a purpose or intended use for the invention." Rowe, 112 F.3d at 478 (Fed.Cir.1997).

In the '325 preamble, the phrase "a memory array in which a plurality of memory circuit devices are arranged" is limiting because "memory array" and "memory circuit devices" provide antecedent basis for "the memory array" and "the memory devices" in part (e) of the body of Claim 1. 8:39-40; 9:7. Further, the phrase provides essential structure to the invention not set forth in the body of the claim. Bicon, Inc., 441 F.3d at 952. However, the remainder of the preamble is not limiting because it describes the claimed invention's purpose or intended use, rather than describing essential structure. *See* 8:40-47; Rowe, 112 F.3d at 478. This segment of the preamble describes how the arrangement of memory devices may allow memory information to be obtained, but it does not describe any essential structure. By contrast, the entire '849 preamble is limiting because it recites essential structure and provides antecedent basis for part (b) of the body of Claim 1. *See* 9:5,7, and 14.

The '328 Patent

Conductive leads for electrically coupling with an electronic device, wherein said conductive leads electrically couple with said conductive traces

There are several points of contention concerning the construction of this claim language, and the Court will address them individually. To begin with, Tessera argues that the entire phrase should be construed, whereas Micron contends only "conductive leads" requires construction.FN4 The Court agrees with Micron that only the phrase "conductive leads" should be construed.

FN4. Micron argues "conductive leads" are "conductive I/O elements on the outside of the body." Tessera argues the entire phrase should be construed to mean "[a]n electrical conductor, made up of electrically conductive material, long and thin, not shaped as a mass, used as input/output (I/O) for connecting the package body to an external device. The conductive leads are connected to the conductive traces to provide an electrical current path between the leads and the traces."

[24] For the purposes of this discussion, the disputed claim language can be roughly broken up into three parts. First, "conductive leads," are identified, then the relationship between the "conductive leads" and the "electronic device" is described, and finally the relationship between the "conductive leads" and the "conductive traces" is described. In each relationship, the "conductive leads" "electrically couple" or are "electrically coupling," with the "conductive traces" and "electronic device," respectively. Properly understood, the entire phrase describes "conductive leads" acting as electrically conductive bridges between the "conductive traces" and the "electronic device." That understanding may be gained from the plain and

ordinary meaning of the language, and even if it were not, the Court would not adopt Tessera's construction because it offers no more guidance than the claim language itself.

Tessera's construction tracks the three part structure described above. In describing the relationship between "conductive leads" and "an electronic device," Tessera's construction provides that "conductive leads" are "used as input/output (I/O) for *connecting* the package body to an external device." *Compare* 8:1-2 ("conductive leads for electronically coupling with an electronic device."). Essentially, Tessera substitutes "connecting" for "electronically coupling," which would not offer much assistance to a juror. *See* Sulzer Textil A.G. v. Picanol N.V., 358 F.3d 1356, 1366 (Fed.Cir.2004).

The construction goes on to say that "[t]he conductive leads are *connected* to the conductive traces (emphasis added)" and then clarifies that the purpose of that connection is "to provide an electrical current path between the leads and the traces." *Compare* 8:2-3 ("conductive leads electronically couple to said conductive traces."). Here, Tessera has broken up the phrase "electrically couple" into two phrases that are longer, but not significantly more helpful, than the phrase itself. Tessera's construction is not incorrect or confusing, but it simply reorganizes the claim language without offering more guidance than the claim language itself, which makes Tessera's construction unhelpful, and therefore, improper. Sulzer, 358 F.3d at 1366.

The Court will now address the parties' arguments regarding the construction of "conductive leads." FN5 The basic disagreement concerns Tessera's requirement that "conductive leads" be "long and thin, not shaped as a mass." FN6 Micron insists that the patent does not restrict the physical shape or size of the "conductive leads," but Tessera argues that Figures 2 and 3 depict "conductive leads" as long and thin, and further argues that one skilled in the art at the time the patent was issued would understand "conductive leads" to be "long and thin, not shaped as a mass." However, the claim language does not explicitly support such a limitation, nor do the specification or extrinsic evidence compel the conclusion that "conductive leads" must take on any particular physical form.

FN5. The Court will construe this term after having considered the parties pre- *Markman* briefing as well as their oral arguments at the *Markman* hearing and the supplemental post- *Markman* briefing.

FN6. Tessera's construction also describes "conductive leads" as "[a]n electrical conductor, made up of electrically conductive material." However, there is little dispute over the fact that "conductive leads" are electrically conductive, therefore, the Court will not address this segment of Tessera's construction.

Claim 11 recites all of the components comprising the logic component, and describes the pathway along which signals will travel between the electrical device and the semiconductor die. 7:29-32; 8:1-3 (describing "a second shelf having conductive traces thereon ... wherein said traces couple with bond pads on the semiconductor die ... conductive leads for electrically coupling with an electronic device, wherein said conductive leads electrically couple with said conductive traces."). The "conductive leads" occupy a portion of that pathway, but their physical characteristics are not mentioned; only the function of the "conductive leads" as a link in the chain between the semiconductor die and the device is referenced. Therefore, a proper understanding of the claim language requires emphasis on the *role* of the "conductive leads" rather than their *form*.

The specification implicitly refers to the "conductive leads" only three times, calling them "input/output (I/O) leads" or just "I/O leads." 2:24-26; 3:57-60; 4:45-48. Like the claim language, the specification focuses on the role "conductive leads" play, rather than their form. 2:24-26 (describing pads on the upper surface of the shelf being electrically coupled with conductive traces which attach to input/output (I/O)

leads); 3:57-60 and 4:45-48 (describing coupling traces with I/O leads by means such as side brazing). Although Figures 2 and 3 depict "conductive leads" as long and thin, the Court declines to read that limitation into the claim. Burke, Inc., v. Bruno Indep. Living Aids, Inc., 183 F.3d 1334, 1341 (Fed.Cir.1999).

Tessera also argues that, without regard to how the term "leads" is used within the patent, the meaning of "lead" was independently established at the time this patent issued, and any person skilled in the art would understand that "leads" were "long and thin, not shaped as a mass." Micron disputes Tessera's understanding, and the Court finds that the extrinsic evidence is not clear enough to support Tessera's limitation.

In support of its limitation, Tessera cites several patents issued around the time the '328 patent was issued that contain embodiments where "leads" are shown as relatively long and thin. However, the fact that these leads are long and thin does not necessarily require that leads in general must be "long and thin, not shaped as a mass." Tessera goes on to argue that the common understanding of "leads" excludes masses, bumps, or balls, pointing out that chip packages employing solder balls are known as "leadless packages" in the packaging industry. Micron counters that the common understanding of the word lead is much more inclusive, citing the 1989 Edition of the Electronic Materials Handbook, which defines "lead" as "[a] conductive path, usually self-supporting. That portion of an electrical component used to connect it to the outside world." Electronic Materials Handbook, Vol. 1 at 1148 (1989). This definition is consistent with the patent's treatment of the "conductive leads," which was based primarily on the function of the "conductive leads" rather than their form. As the extrinsic evidence is conflicted, the Court is reluctant to rely on that evidence to justify Tessera's more restrictive construction of "conductive leads." Phillips, 415 F.3d at 1318 (Noting that extrinsic evidence is "less reliable than the patent and its prosecution history in determining how to read claim terms.")

The last point of contention concerns Micron's use of the phrase "on the outside of the body." Tessera objects to this language on the basis that "conductive leads" cannot be, at once, a part of a body and outside of that body. The Court disagrees with the logic underlying Tessera's argument, and finds that the additional language is consistent with the claim language and specification. The claim language describes a self-contained die package with "conductive leads *for* coupling with an electronic device (emphasis added)." The electronic device is separate from the claimed logic component, and the leads couple the package with the outside device. Thus, in order to couple with a separate device, it is seemingly necessary that the leads be on the outside of the body. The specification reinforces this understanding of the placement of the conductive leads. 3:57-59 ("the traces have means for coupling with I/O leads on the outside of the ceramic body."); 4:45-47 ("The traces have means for coupling with I/O leads on the outside of the body). Accordingly, the Court construes 'conductive leads' to mean 'conductive input/output' (I/O) elements on the outside of the body."

Conclusion

For the foregoing reasons, the Court interprets the claim language in this case in the manner set forth above. For ease of reference, the Court's claim interpretations are set forth in a table attached to this opinion.

So ORDERED.

JOINT CLAIM CONSTRUCTION CHART
***Micron v. Tessera,* No. 2:05-cv-319**

	Plaintiff's Proposed	Defendant's Proposed	Court's

	Construction	Construction	Construction
Claims 30, 32, and 33			
U.S. Patent No. 6,268,649			
30. A stackable ball grid array package, comprising:			
a **printed circuit board substrate** having a first surface, a second surface, an	**"printed circuit board substrate":**	**"printed circuit board substrate":**	**"printed circuit board substrate":**
aperture therethrough, and a plurality of conductive element pads on said second surface;	**[AGREED]**	**[AGREED]**	A rigid substrate.
at least one semiconductor device mounted within a first perimeter of said first surface of said **printed circuit board substrate**, said at least one semiconductor device having a plurality of bond pads on a first surface thereof;			
a plurality of wire bonds connecting at least some of said plurality of conductive element pads and some of said plurality of bond pads on said second surface of said **printed circuit board substrate** and extending through said aperture in said **printed circuit board substrate**;			
encapsulant placed along a portion of said aperture, said plurality of bond pads, and said plurality of wire bonds, said encapsulant forming a first profile height; and			
a plurality of conductive elements mounted along a second perimeter of said second surface, said second perimeter being greater than said first perimeter, said plurality of conductive elements connected to some of said plurality of conductive element pads on said second surface, said plurality of conductive elements having a second profile height of one of a height greater than said first profile height and a height substantially equal to said first profile height.			
32. The stackable ball grid array package according to claim 30, wherein a first portion of said plurality of conductive elements aligns in a substantially parallel row having a first pitch spacing.			
33. The stackable ball grid array package according to claim 32, wherein a second portion of said plurality of conductive			

elements aligns in a second parallel row having a second pitch spacing.			
Claims 6 and 7			
U.S. Patent No. 6,013,948			
6. A stackable semiconductor package comprising:			
a **substrate** comprising a first surface, an opposing second surface, and **a cavity;**	**"substrate":** **[AGREED]**	**"substrate":** **[AGREED]**	**"substrate":** A supporting material.
a plurality of first contacts on the first surface;	**"cavity":**	**"cavity":**	
a plurality of second contacts on the second surface, the second contacts configured for electrically engaging third contacts substantially identical to the first	**[AGREED]**	**[AGREED]**	No construction.
contacts on a second semiconductor package substantially identical to the semiconductor package;	**"plurality of conductive vias":**	**"plurality of conductive vias":**	**"plurality of conductive vias"**:
a **plurality of conductive vias** in the **substrate** electrically connecting the first contacts to the second contacts; and	**[AGREED]**	**[AGREED]**	Through holes with conductive material that permit electrical connections.
a semiconductor die comprising a plurality of die contacts, the die **mounted to** the cavity at least partially encapsulated in a	**"mounted to the cavity":**	**"mounted to the cavity":**	
polymer within the **cavity** with the die contacts in electrical communication with the first contacts or the second contacts.	**[AGREED]**	**[AGREED]**	No construction.
7. The package of claim 6 wherein the **substrate** comprises silicon and the **conductive vias** comprise electrically insulated openings at least partially filled with a conductive material.	**"substrate":** **[AGREED]**	**"substrate":** **[AGREED]**	**"substrate":** A supporting material.
	"conductive vias": **[AGREED]**	**"conductive vias":** **[AGREED]**	**"conductive vias":** Through holes with conductive material that permit electrical connections.
Claims 25-27 and 29-30			
U.S. Patent No. 5,739,585			
25. A semiconductor package comprising:			
a package body comprising **a resin-glass laminate** with an elongated opening	**"a resin-glass laminate":**	**"a resin-glass laminate":**	**"a resin-glass laminate":**

there through, said body including a first surface and an opposed second surface;	**[AGREED]**	**[AGREED]**	A multilayer material including resin and glass.
a semiconductor die comprising a circuit side with a plurality of bond pads, said circuit side attached to the first surface with an adhesive layer therebetween, and with the bond pads on the die in alignment with the opening;			
a pattern of conductors formed on the second surface of the package body, at least one of said conductors including a metal ball;			
a plurality of wires placed through the opening and bonded to the bond pads and conductors; and			
a **curable material** placed within the opening to encapsulate at least	**"curable material":**	**"curable material":**	**"curable material":**
a portion of the wires.	**[AGREED]**	**[AGREED]**	A substance that may be hardened.
26. The package as claimed in claim 25 wherein the **curable material** comprises	**"curable material":**	**"curable material":**	**"curable material":**
a material selected from the group consisting of epoxy, silicone, polyimide, and a room temperature vulcanizing material.	**[AGREED]**	**[AGREED]**	A substance that may be hardened.
27. The package as claimed in claim 25 further comprising **a solder mask** formed	**"a solder mask":**	**"a solder mask":**	**"a solder mask":**
on the conductors for attaching a plurality			
of solder bumps to the conductors.	**[AGREED]**	**[AGREED]**	A coating that is formed on a conductor that leaves exposed areas where solder is to be attached or added.
29. The package as claimed in claim 25 wherein the **resin-glass laminate comprises a FR-4 material.**	**"a resin-glass laminate":**	**"a resin-glass laminate":**	**"a resin-glass laminate":**
	[AGREED]	**[AGREED]**	A multilayer material including resin and glass.
30. The package as claimed in claim 25 wherein a plurality of dice are mounted to the first surface to form a multi chip module.			
Claims 1-3 and 10-11			
U.S. Patent No. 5,107,328			
1. A body for receiving a semiconductor	**"lid":**	**"lid":**	

die, said body comprising: a) a first shelf for receiving a **lid**; b) a **second shelf having conductive traces thereon, said second shelf overlying a portion of the semiconductor die, wherein said traces couple with bond pads on the semiconductor die;** c) a third shelf for receiving a **base**; and d) **conductive leads for electrically coupling with an electronic device, wherein said conductive leads electrically couple with said conductive traces**.	**[AGREED]**	**[AGREED]**	No construction.
	"second shelf having conductive traces thereon, said second shelf overlying a portion of the semiconductor die, wherein said traces couple with bond pads on the semiconductor die":	**"second shelf having conductive traces thereon, said second shelf overlying a portion of the semiconductor die, wherein said traces couple with bond pads on the semiconductor die":**	
	[AGREED]	**[AGREED]**	The second shelf, and the conductive traces on the second shelf, cover a portion of the semiconductor die wherein said traces electrically couple the bond pads on the semiconductor die and the conductive traces on the second shelf.
	Tessera did not request separate construction of "shelf" and "conductive traces" at the time specified by PR 4-1 or PR 4-2.	**"shelf"**: The parties both agree that this term does not need to be construed separately. However, if the Court concludes that this term requires construction, the parties disagree as to how this term should be construed. Tessera believes that it should be construed to mean: A thin, flat, long, and narrow piece of material extending	No construction.

		horizontally at a distance from a base to hold objects. *See* Tessera's Responsive Claim Construction Brief at 19-20.	
		"conductive traces": The parties both agree that this term does not need to be construed separately. However, if the Court concludes that this term requires construction, the parties disagree as to how this term should be construed. Tessera believes that it should be construed to mean: Long strips of metal formed on the second shelf that connect one end of the bond wire to the conductive leads. See Tessera's Responsive Claim Construction Brief at 19-21	No construction.
	"base":	**"base":**	
	[AGREED]	**[AGREED]**	No construction.
	"conductive leads for electrically coupling with an electronic device, wherein said conductive leads electrically couple with said conductive traces":	**"conductive leads for electrically coupling with an electronic device, wherein said conductive leads electrically couple with said conductive traces":**	
	Conductive I/O elements on the outside of the	An electrical conductor, made up of electrically	Conductive leads: conductive input/output

	body.	conductive material, long and thin, not shaped as a mass, used as input/output (I/O) for connecting the package body to an external device. The conductive leads are connected to the conductive traces to provide an electrical current path between the leads and the traces.	(I/O) elements on the outside of the body. No construction for the remainder of the disputed phrase.
2. The body of claim 1, wherein said second shelf contains a void, said void being located approximately above the bond pads of the semiconductor die, wherein a conductive material passes through said void to electrically couple said conductive traces with the bond pads on the semiconductor.			
3. The body of claim 2, wherein said void bisects said second shelf.			
10. The body of claim 1 wherein said body is manufactured from a material comprising plastic.			
11. A logic component comprising: a) a semiconductor die; b) a body for receiving	**"lid":**	**"lid":**	
said semiconductor die; c) a **lid** and a **base** receivable by said body;	**[AGREED]**	**[AGREED]**	No construction.
d) a first shelf for receiving said **lid**; e) a **second shelf having conductive traces thereon, said second shelf overlying a portion of the semiconductor die, wherein said traces couple with bond pads on the semiconductor die;** f) a third shelf for receiving said **base**; and	**"base":** **[AGREED]**	**"base":** **[AGREED]**	No construction.
g) **conductive leads for electrically coupling with an electronic device, wherein said conductive leads electrically couple with said conductive traces.**	**"second shelf having conductive traces thereon, said second shelf overlying a portion of the semiconductor die, wherein said traces couple with bond pads on the semiconductor die":** **[AGREED]**	**"second shelf having conductive traces thereon, said second shelf overlying a portion of the semiconductor die, wherein said traces couple with bond pads on the semiconductor die":** **[Agreed]**	The second shelf, and

			the conductive traces on the second shelf, cover a portion of the semiconductor die wherein said traces electrically couple the bond pads on the semiconductor die and the conductive traces on the second shelf.
	Tessera did not request separate construction of "shelf" and "conductive traces" at the time specified by PR 4-1 or PR 4-2.	**"shelf"**: The parties both agree that this term does not need to be construed separately. However, if the Court concludes that this term requires construction, the parties disagree as to how this term should be construed. Tessera believes that it should be construed to mean: A thin, flat, long, and narrow piece of material extending horizontally at a distance from a base to hold objects. See Tessera's Responsive Claim Construction Brief at 19-20.	No construction.
		"conductive traces": The parties both agree that this term does not need to be construed separately. However, if the Court concludes that this term requires construction, the parties disagree as to how this term should be construed. Tessera believes that it should be construed to	No construction.

		mean: Long strips of metal formed on the second shelf that connect one end of the bond wire to the conductive leads. See Tessera's Responsive Claim Construction Brief at 19-21.	
	"conductive leads for electrically coupling with an electronic device, wherein said conductive leads electrically couple with said conductive traces":	**"conductive leads for electrically coupling with an electronic device, wherein said conductive leads electrically couple with said conductive traces":**	
	Conductive I/O elements on the outside of the body.	An electrical conductor, made up of electrically conductive material, long and thin, not shaped as a mass, used as input/output (I/O) for connecting the package body to an external device. The conductive leads are connected to the conductive traces to provide an electrical current path between the leads and the traces.	Conductive leads: conductive input/output (I/O) elements on the outside of the body. No construction for the remainder of the disputed phrase.
Claims 35 and 43			
U.S. Patent No. 6,265,766			
35. An electrical assembly for connection to a substrate having a plurality of	**"bare semiconductor die":**	**"bare semiconductor die":**	**"bare semiconductor die":**
circuits comprising: a **bare semiconductor die** having a surface having a plurality of **bond pads** located thereon; a die	**[AGREED]**	**[AGREED]**	At least one face of the semiconductor is exposed.
substrate having a die side surface, an attachment surface,	**"bond pads":**	**"bond pads":**	**"bond pads":**
a **via extending through the die substrate** from the die side surface to	**[AGREED]**	**[AGREED]**	A conductive surface to which a wire bond is

the attachment surface, and a plurality of circuit traces, a portion of the surface having the plurality of bond pads of said **bare semiconductor die** attached to a portion of the die side surface of the die substrate; a plurality of wire bonds extending			attached.
through the **via extending through the die substrate** from the die side surface to the attachment surface	**"via extending through the die substrate":**	**"via extending through the die substrate":**	**"via extending through the die substrate":**
thereof, the plurality of wire bonds connected to the plurality of bond pads of the **bare semiconductor die** and the plurality of circuit traces; and a plurality of electrical connectors located on the attachment surface of the die substrate for electrically connecting the die substrate and said substrate, the plurality of electrical connectors connected to the plurality of circuit traces.	**[AGREED]**	**[AGREED]**	A hole that extends from one surface on the die substrate to the opposite surface.
43. The electrical assembly of claim 35, where the die substrate comprises a printed circuit board.			
Claims 1-2, 8, and 10-11			
U.S. Patent No. Re 36,325			
1. **A memory array in which a plurality of memory circuit devices are arranged in a manner such that memory information is obtained by addressing bits of information from a selected number of the memory devices in the array in a format, and the format of bits forms a byte of memory data such that each byte includes bits from each memory device in the selected number of the circuit devices, and wherein the bits are addressed as rows and columns of information in a matrix on each memory device, characterized by:**	**This claim is not a Jepson claim.** **The preamble of this claim is not a limitation.**	**This claim is a Jepson claim wherein the preamble is admitted prior art, and all of the elements set forth therein must be present in an accused device to establish infringement.**	This claim is not a Jepson claim. The preamble of this claim is a limitation as discussed in the Court's claim construction opinion.
(a) a support structure which includes a single polymeric sheet, the polymeric sheet having a plurality of die receiving portions thereon, having tape automated bond (TAB) leads thereon and having a first set of electrical circuit traces on one side of the polymeric sheet, the tape automated bond pads being in electrical communication with the circuit traces;			
(b) a plurality of integrated circuitry			

memory devices, each device consisting of circuit elements deposited on a substrate and having conductive bumps deposited thereon, the integrated circuit devices being located within separate ones of the receiving portions of the single polymeric sheet,			
and connected to the polymeric sheet by being attached to the tape automated bond pads at the conductive bumps, and each of the integrated circuit devices being connected to the TAB leads on the polymeric sheet within its respective die receiving portion;	**"means to mechanically stabilize the memory array so that the polymeric sheet, the memory devices and the circuit terminals are maintained in**	**"means to mechanically stabilize the memory array so that the polymeric sheet, the memory devices and the circuit terminals are maintained in**	
(c) a second set of circuit traces on a plane which is separate from said one side of the polymeric sheet, the second set of circuit traces being in electrical communication	**electrical communication during normal service"**	**electrical communication during normal service"**	
with the first set of electrical circuit traces;	**Claimed function:**	**Claimed function:**	
(d) circuit terminals in electrical communication with the circuit traces, the circuit terminals configured in a pattern which conforms to a predetermined external circuit connection and memory address protocol; and	**[AGREED]**	**[AGREED]**	**Claimed function:** to mechanically stabilize the memory array so that the polymeric sheet, the memory devices and the circuit terminals are maintained in electrical communication during normal service
(e) **means to mechanically stabilize the memory array so that the polymeric sheet, the memory devices and the circuit terminals are maintained in electrical communication during normal service.**	**Corresponding structure:**	**Corresponding structure:**	**Corresponding structure:**
	[AGREED]	**[AGREED]**	"Resin"
2. A memory array as defined in claim 1, further characterized by: the means to mechanically stabilize the memory array including mechanical structure which			
8. A memory array as described in claim 1, characterized by:			
(a) each memory device having addresses which are arranged in similar matrices of rows and columns on the memory device; and			
(b) the addressing of a row of memory			

devices being accomplished to corresponding rows and columns on each memory device in a row of memory devices in response to address commands.			
10. A memory array as described in claim 1, further characterized by:			
(a) the memory devices being random access memory semiconductor devices, having read and write address bits thereon;			
(b) the devices having row and column enable bits for the memory devices.			
11. A memory array as described in claim 1, further characterized by: the memory devices being dynamic random access memories.			
Claims 1, 2, 8, 10-11			
U.S. Patent No. 4,992,849			
1. **Board level integrated circuit in which a plurality of semiconductor circuit devices are arranged on a flexible circuit board and each of the semiconductor circuit devices is a distinct integrated circuit chip, characterized by:**	**This claim is not a Jepson claim. The preamble of this claim is not a limitation.**	**This claim is a Jepson claim wherein the preamble is admitted prior art, and all of the elements set forth therein must be present in an accused device to establish infringement.**	This claim is not a Jepson claim. The preamble of this claim is a limitation as discussed in the Court's claim construction opinion.
(a) a support structure which includes a single polymeric sheet, the polymeric sheet having a plurality of die receiving portions thereon, having tape automated bond (TAB) pads thereon and having a first set of electrical circuit traces on one side of the polymeric sheet, the tape automated bond pads being in electrical communication with the circuit traces;			
(b) the plurality of integrated circuit devices each consisting of circuit elements deposited on a substrate and having conductive bumps deposited thereon, the integrated circuit devices being located within			
separate ones of the die receiving portions of the single polymeric sheet, mounted to the polymeric sheet and connected to the polymeric sheet by being attached to the tape automated bond pads at the conductive bumps, and each of the integrated circuit devices being connected to the TAB leads on the polymeric sheet within its respective die	**"means to mechanically stabilize the polymeric sheet with the integrated circuit devices mounted thereon so that the polymeric sheet, the integrated**	**"means to mechanically stabilize the polymeric sheet with the integrated circuit devices mounted thereon so that the polymeric sheet, the integrated**	

receiving portion; (c) a second set of circuit traces on a plane which is separate from said one side of the polymeric sheet, the second set of circuit traces being in electrical communication with the first set of electrical circuit traces; (d) circuit terminals in electrical communication with the circuit traces, the circuit terminals configured in a pattern which conforms to a predetermined external circuit connection protocol; and (e) **means to mechanically stabilize the polymeric sheet with the integrated circuit devices mounted thereon so that the polymeric sheet, the integrated circuit devices and the circuit terminals are maintained in electrical communication during normal service.**	**circuit devices and the circuit terminals are maintained in electrical communication during normal service"** **Claimed function:** **[AGREED]** **Corresponding structure:**	**circuit devices and the circuit terminals are maintained in electrical communication during normal service"** **Claimed function:** **[AGREED]** **Corresponding structure:**	**Claimed function**: to mechanically stabilize the polymeric sheet with the integrated circuit devices mounted thereon so that the polymeric sheet, the integrated circuit devices and the circuit terminals are maintained in electrical communication during normal service. **Corresponding structure:**
	[AGREED]	**[AGREED]**	"Resin"
2. Board level integrated circuit as defined in claim 1, further characterized by: the means to mechanically stabilize the board level integrated circuit including mechanical structure which supports the circuit terminals.			
8. Board level integrated circuit as described in claim 1, characterized by: (a) **a group of the integrated circuit devices** having addresses which are arranged in similar matrices of rows and columns on the integrated circuit device; and	**"a group of the integrated circuit devices":**	**"a group of the integrated circuit devices":**	**"a group of the integrated circuit devices":**
(b) the addressing of a row of integrated circuit devices in the group being accomplished to corresponding rows and columns on each integrated circuit device in a row of integrated circuit devices in the group in response to address commands.	**[AGREED]**	**[AGREED]**	Two or more integrated circuit devices.
10. Board level integrated circuit as described in claim 9, further characterized			

by: the integrated circuit devices being dynamic random access memories.			
11. Board level integrated circuit as described in claim 1, further characterized by:			
a group of the integrated circuit devices being random access memory semiconductor devices, having read and write address bits thereon, having row and column enable bits for the memory devices.	**"a group of the integrated circuit devices":**	**"a group of the integrated circuit devices":**	**"a group of the integrated circuit devices":**
	[AGREED]	**[AGREED]**	Two or more integrated circuit devices.

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