United States District Court,
N.D. California.

HYNIX SEMICONDUCTOR INC., Hynix Semiconductor America Inc., Hynix Semiconductor U.K. Ltd., and Hynix Semiconductor Deutschland GmbH,
Plaintiffs.
v.
RAMBUS INC,
Defendant.

No. CV-00-20905 RMW

Nov. 15, 2004.

Kenneth L. Nissly, Susan van Keulen, Geoffrey H. Yost, Thelen Reid & Priest LLP, San Jose, CA, Theodore G. Brown, III, Townsend & Townsend & Crew LLP, Palo Alto, CA, Patrick Lynch, Kenneth R. O'Rourke, O'Melveny & Myers, Los Angeles, CA, for plaintiff.

Gregory P. Stone, Kelly M. Klaus, Andrea W. Jeffries, Munger Tolles & Olson, Los Angeles, CA, for defendant.

CLAIM CONSTRUCTION ORDER

WHYTE**, J.**

At issue is the construction of disputed terms used in 15 patents descending from a single patent application, U.S. Patent Appl. No. 07/510,898 ("the '898 application"). Defendant Rambus Inc. and plaintiffs Hynix Semiconductor Inc., Hynix Semiconductor America Inc ., Hynix Semiconductor U.K. Ltd., and Hynix Semiconductor Deutschland Gmbh ("Hynix") briefed the issues and presented evidence at a claim construction hearing on March 23, 2004. The court has read the moving and responding papers, including the patents-in-suit and the relevant prosecution history, considered the arguments of counsel, and now construes the disputed terms in the claims.

I. BACKGROUND

A. Factual background

Rambus is the assignee of several patents covering Synchronous Dynamic Random Access Memory ("SDRAM") chips and related interface and memory control technology. Second Am. Compl. para. 10. In the vast majority of computers, Dynamic Random Access Memory ("DRAM") serves as the main memory for temporary storage of data currently being utilized by the Central Processing Unit ("CPU" or "processor"). In contrast to a hard drive, which permits long-term "non-volatile" storage, DRAMs do not retain information written to them once the computer is turned off. FN1 Information on a hard drive, however, must be transferred to a main memory composed of DRAM before it can be accessed by the CPU. Thus, in most computers, a main memory composed of DRAM is the principal storage location for computer programs that are running at a given time, along with the data on which the programs operate.

FN1. DRAMs lose their contents once power is no longer applied to the circuit because each bit is stored as

a charge in a memory cell composed of a transistor and a capacitor. While a system is running the charge that creates each bit deteriorates. As a result, all DRAM memory locations must periodically have their charges refreshed.

DRAMs are generally arranged in two-dimensional arrays of memory cells designated by rows and columns. Exactly one bit of information is stored at each row-column intersection. An individual datum stored in the array is accessed by supplying the DRAM with the row and column address corresponding to the location of the memory cell to be accessed. Control information instructs the DRAM on what operation is to be performed. Basic operations include read accesses, where data is retrieved from the DRAM cells, and write operations, where data is written to selected cells.

The patented inventions deal with computer memory devices called Synchronous DRAM ("SDRAM"). SDRAM is a type of memory designed to improve the speed and efficiency of data transfers to and from devices that access the memory. In most operational circumstances, when appropriately designed for use in a general purpose computer, SDRAM devices provide a performance advantage over earlier DRAM devices. The initial Rambus application was the '898 application filed on April 18, 1990. Rambus asserts that the SDRAM patents are entitled to that date as their effective filing date. Rambus claims patents for "the interface circuitry that connects DRAMs to the CPUs with which they communicate and that connects them to the overall systems in which they reside." Def.'s Opening Claim Const. Br. ("CC Brief") at 3. Rambus claims eleven distinct groups of inventions stemming from the '898 application. Each of these claimed inventions addresses a "memory bottleneck" problem, where a busmaster FN2 normally has to wait for data to be available for transfer to or from the DRAM. FN3 Specifically, Rambus contends that by using its invention, DRAMs are able to provide data to a busmaster as fast as that processor can process it, thus keeping pace with the ever-increasing speed of CPUs. Each patent in suit describes the same field of invention:

FN2. Initiators of data transfers are called busmasters.

FN3. Rambus asserts that using all eleven inventions results in the most effective speed and efficiency but that each invention may be used individually or in combination. CC Br. at 5.

An integrated circuit bus interface for computer and video systems ... which allows high speed transfer of blocks of data, particularly to and from memory devices, with reduced power consumption and increased system reliability. A new method of physically implementing the bus architecture is also described.
U.S. Patent No. 5,953,263 ("the '263 patent"), col. 1, ll. 9-15.FN4
FN4. Hynix references to the Rambus patent specification are to U.S. Patent No. 6,101,152 ("the '152 patent"); Rambus references the '263 patent. For ease of citation, all references to the specification will be to the '263 patent.

In the 1990's, the Joint Electronic Devices Engineering Council ("JEDEC") coordinated the development of technology standards for SDRAM chips. Second Am. Compl. para. 12. Plaintiff alleges, *inter alia,* that as a member of JEDEC, Rambus used information gained from the standards-setting process to secretly and fraudulently secure the patents at issue ("SDRAM patents"), and, therefore, market power. Plaintiff further alleges that these actions were taken in violation of JEDEC's rules and various federal and state laws. Second Am. Com pl. para.para. 11-13.FN5

FN5. Plaintiff also apparently alleges that Rambus disparaged technology standards for chips that would not be covered by Rambus's patents.

B. Legal background

Certain terms in the same family of disputed patents have already been construed by the Eastern District of Virginia in Rambus, Inc. v. Infineon Techs. AG, 2001 WL 34138091 (E.D.Va.2001) ("*Infineon I*"). Specifically, the terms "bus," "block size information," "read request," "write request," "transaction request," "first external clock signal," "second external clock signal" and "integrated circuit device" were construed in *Infineon I*. The district court in *Infineon I* granted summary judgment of non-infringement for Infineon, entered judgment on a jury verdict of fraud under Virginia state law for conduct occurring during JEDEC SDRAM standardization proceedings, and granted judgment as a matter of law in favor of Rambus, overturning a jury verdict of fraud committed during consideration of DDR-SDRAM standards. FN6 Rambus, *inter alia,* appealed the district court's claim construction of the terms "integrated circuit device," "read request," "write request," "transaction request," and "bus." *See* Rambus, Inc. v. Infineon Techs. AG, 318 F.3d 1081, 1088 (Fed.Cir.2003) ("*Infineon II*"). The Federal Circuit reversed the district court and disagreed with the district court's construction of each of these terms, vacated the judgment of noninfringement, vacated the jury's SDRAM fraud verdict, and remanded for further proceedings under the revised claim construction. *See* id. at 1106. Of these terms, the parties dispute only the proper construction of "integrated circuit device."

FN6. The district court found that substantial evidence did not support the jury's verdict because Rambus left JEDEC before work officially began on the DDR-SDRAM standard. *See* Rambus, Inc. v. Infineon Techs. AG, 164 F.Supp.2d 743, 767 (E.D.Va.2001).

On November 21, 2001 this court granted plaintiff's motion for partial summary judgment of non-infringement with respect to twenty-seven claims from the patents-in-suit. In its November 2001 order, the court concluded that the doctrine of collateral estoppel barred Rambus from re-litigating claim construction and infringement of certain representative claims of the patents-in-suit. The court's earlier order was based on the claim construction and judgment of non-infringement entered against Rambus in *Infineon I*. In light of the Federal Circuit's January 29, 2003 order reversing *Infineon I*' s construction of certain terms in the asserted claims, the court on July 25, 2003 vacated in its entirety the November 21, 2001 order.

II. ANALYSIS

The construction of patent claim terms is a matter of law for the court. Markman v. Westview Instruments, Inc., 517 U.S. 370, 372, 116 S.Ct. 1384, 134 L.Ed.2d 577 (1996) ("*Markman II*"). As the language of the claim defines the scope of the claim, claim construction analysis begins with the words of the claim. Teleflex, Inc. v. Ficosa N. Am. Corp., 299 F.3d 1313, 1324 (Fed.Cir.2002); ASM Am., Inc. v. Genus, Inc., 260 F.Supp.2d 827, 831 (N.D.Cal.2002). "As a general rule, claim language carries the meaning of the words in their normal usage in the field of the invention." Infineon II, 318 F.3d at 1088 (citing Toro Co. v. White Consol. Indus., Inc., 199 F.3d 1295, 1299 (Fed.Cir.1999)). In other words, claim language is construed to mean "what one of ordinary skill in the art at the time of the invention would have understood the term to mean." *Id* . (quoting Markman v. Westview Instruments, Inc., 52 F.3d 967, 986 (Fed.Cir.1995) ("*Markman I*")).

However, where the intrinsic evidence shows that the specification uses the words in a manner clearly inconsistent with their ordinary meaning, the ordinary meaning must be rejected. *See* Tex. Digital Sys., Inc. v. Telegenix, Inc., 308 F.3d 1193, 1204 (Fed.Cir.2002). In short, "inventors may act as their own lexicographers and use the specification to supply implicitly or explicitly new meanings for claim terms." Infineon II, 318 F.3d at 1088. Nevertheless, where a patentee has elected to be a lexicographer by providing a definition in the specification for a claim term, the patentee's lexicography must appear "with reasonable

clarity, deliberateness, and precision." Renishaw PLC v. Marposs Societa' Per Azioni, 158 F.3d 1243, 1249 (Fed.Cir.1998) (quoting In re Paulsen, 30 F.3d 1475, 1480 (Fed.Cir.1994)). If the patentee provides such a clear definition, reference to the written description is required, "because only there is the claim term defined as it is used by the patentee." *Id*. Thus, claim construction is guided by two fundamental, sometimes conflicting, canons: "(a) one may not read a limitation into a claim from the written description, but (b) one may look to the written description to define a term already in a claim limitation, for a claim must be read in view of the specification of which it is a part." Renishaw, 158 F.3d at 1248 (citing Vitronics Corp. v.. Conceptronic, Inc., 90 F.3d 1576, 1582 (Fed.Cir.1996)); Markman I, 52 F.3d at 979-80.

Notably, "it is manifest that a claim must explicitly recite a term in need of definition before a definition may enter the claim from the written description." Renishaw, 158 F.3d at 1248. "The intrinsic evidence, and, in some cases, the extrinsic evidence, can shed light on the meaning of the terms recited in a claim, either by confirming the ordinary meaning of the claim terms or by providing special meaning for claim terms." *Id*. (citing Vitronics, 90 F.3d at 1583).

Consulting the written description and prosecution history prior to ascertaining the ordinary meaning "invites a violation of our precedent counseling against importing limitations into the claims." Texas Digital, 308 F.3d at 1204 (citations omitted). Rather, the full breadth of the limitations intended by the inventor will be more accurately guided by examining relevant dictionaries, encyclopedias and treatises "publicly available at the time the patent is issued...." Id. at 1203. "Such references are unbiased reflections of common understanding not influenced by expert testimony or events subsequent to the fixing of the intrinsic record by the grant of the patent, not colored by the motives [of] the parties, and not inspired by litigation." *Id*. Examining these references together with the intrinsic evidence allows a court to construe terms more consistently with the inventor's use of the terms, more accurately determine the full breadth of the limitations, and avoid the improper importation of unintended limitations from the written description into the claims. *Id*. at 1205.

Since the Federal Circuit has already construed certain claim terms, these constructions are done as a matter of law and are given *stare decisis* effect. *See Markman II,* 417 U.S. at 390; Cybor Corp. v. FAS Tech., Inc., 138 F.3d 1448, 1455 (Fed.Cir.1998) (noting that in *Markman II* "the Supreme Court endorsed this court's role in providing national uniformity to the construction of a patent claim."); Key Pharm. v. Hercon Labs. Corp., 161 F.3d 709, 716 (Fed.Cir.1998).

1. Device

a. Proposed constructions

Hynix asserts that "device" should be construed as "[e]lectronic circuits or components physically connected in a unit, with an interface to a bus having a multiplexed set of signal lines used to transmit substantially all address, data, and control information, and containing substantially fewer lines than the number of bits in a single address." Hynix contends that the definition of "device" is a common denominator in several terms, and, therefore, should be separately defined and incorporated into each of the asserted claims.

Rambus counters that "device," by itself, is not a proper term for construction. Specifically, it contends that although the word "device" does appear in the claims, it only appears in conjunction with other terms, *i.e*. "integrated circuit device," "memory device," and "synchronous memory device." Rambus argues that it would be improper for the term "device" to be construed separately from the context in which it appears in the claims. Thus, Rambus argues that only "integrated circuit device," "memory device" and "synchronous memory device" should be construed. Rambus also submits that Hynix's proffered construction of "device" would read multiplexing into the claims, and that such a construction would be at odds with the Federal Circuit's decision.

b. Federal Circuit

The Federal Circuit reversed *Infineon I*' s construction of "bus" to mean "a multiplexed set of signal lines used to transmit address, data and control information." Infineon II, 318 F.3d at 1094.FN7 The district court held that the patentees acted as their own lexicographer by redefining "bus" to mean a "multiplexed bus." When the Federal Circuit overturned this construction, it noted that "[t]he claims do not specify that the bus multiplexes address, data and control information. *See* '918 patent, col. 26, ll. 19-27. Nothing in the claims compels a definition different from the ordinary meaning of 'bus." ' Id.

FN7. In the context of this patent family "[m]ultiplexing refers to the sharing of a single set of lines to send multiple types of information." Infineon II, 318 F.3d at 1094. The multiple types of information under the district court's construction included address, data and control information.

The Federal Circuit acknowledged that the Summary of the Invention and Detailed Description in the specification supported an inference that "bus" was limited to a multiplexing bus, but went on to note that "the remainder of the specification and prosecution history shows that Rambus did not clearly disclaim or disavow such claim scope in this case." Infineon II, 318 F.3d at 1094-95 (citing Inverness Med. Switz. GmbH v. Princeton Biomeditech Corp., 309 F.3d 1365, 1372 (Fed.Cir.2002) (statements made during prosecution not clear and unambiguous disclaimer of claim scope)). The Federal Circuit found that multiplexing was not a requirement in all of Rambus's claims. Specifically, at least two original claims of the '898 application recite a multiplexed bus, while others do not.FN8 In addition, the court of appeals reasoned that Rambus distinguished certain claims as reciting a multiplexed bus because Rambus viewed "bus" as having its ordinary meaning. "Indeed, it is because Rambus viewed 'bus' under its ordinary meaning that Rambus specified-in the claim language-that the inventive multiplexing bus carries substantially all address, data, and control information and that the bus operates without the need for device-select lines." *Id*. at 1095.

FN8. For example, original claim 1 of the '898 application recites a "bus including a plurality of bus lines for carrying substantially all address, data and control information needed by said memory device." Infineon II, 318 F.3d at 1095. Other original claims require that the "bus carry ... device-select information without the need for separate device-select lines connected directly to individual semiconductor devices." *Id*.

The Federal Circuit also noted that, in prosecuting the claims of U.S. Patent No. 5,841,580 ("the '580 patent"), the parent of the '263 patent, "the PTO issued a two-way restriction, dividing the claims into two distinct groups: a multiplexing bus group (Group I) and a latency invention group (Group II)." Id. at 1095. "Rambus elected to prosecute the latency claims from Group II in the '580 patent. Therefore, the claims of the '580 patent do not require a multiplexing bus." Id. As the claims of the '580 patent recite a bus, the court of appeals concluded that the PTO understood that "bus" was not limited to a multiplexing bus. Id. "The specification and prosecution histories, taken in their entirety, convince this court that Rambus did not redefine 'bus' to be a multiplexing bus in the patents-in-suit." Id. "[T]he term 'bus' carries its ordinary meaning as a set of signal lines to which a number of devices are connected, and over which information is transferred between devices." Id. at 1095.

Here, rather than applying a multiplexing limitation to the bus, Hynix asserts that multiplexing should limit the term "device." It remains unclear how "[e]lectronic circuits or components physically connected in a unit, with an interface to a bus having a multiplexed set of signal lines" is materially different from limiting the term "bus" to a "multiplexed bus." Although the focus is on the memory chip itself rather than its operational means of connection to the bus, the end result remains the same-the bus upon which the devices reside in the patents at issue would necessarily be a multiplexed bus. This end result, a multiplexed bus as part of the claim limitations, was rejected by the Federal Circuit.

Hynix relies on the Summary of the Invention, the Detailed Description, and the recitation of the objects of the invention in support of its contention that Rambus has acted as its own lexicographer in defining "device." This is largely the same material in the specification that the Federal Circuit found inadequate to support the multiplexing limitation on the term "bus." *See* Infineon II, 318 F.3d at 1094-95. In addition, U.S. Patent No. 6,101,152 ("the '152 patent") descends from the same '580 patent that does not require a multiplexing bus. The court, therefore, does not read a multiplexed bus limitation into the term "device." "Device" must be construed in the context of "integrated circuit device," "memory device," or "synchronous memory device."

2. Integrated Circuit Device

a. Proposed constructions

Rambus requests that this court adopt the Federal Circuit's construction of "integrated circuit device," as "a circuit constructed on a single monolithic substrate, commonly called a 'chip.' ' CC Br. at 14; Infineon II, 318 F.3d at 1091. Hynix proposes that "integrated circuit device" be construed as "a device that includes one or more integrated circuits."

b. Federal Circuit

The district court in *Infineon I* construed "integrated circuit device" in the related U.S. Patent No. 5,954,804 ("the '804 patent) as requiring "a device ID register, interface circuitry and comparison circuitry." 2001 WL 34138091 at *28. Hynix contends that the Federal Circuit's construction of integrated circuit device was dictum not essential to its decision. Specifically, Hynix argues that here, limiting integrated circuit device as including an "identification register" is not at issue.

The Federal Circuit examined the language of claim 26 of the '804 patent FN9 and found that the claim language did not support the district court's construction, noting that the terms "comparison circuitry" and "device identification register" do not appear anywhere in the text of the claim. Infineon II, 318 F.3d at 1089. The Federal Circuit also noted that there was "no justification for reading unstated limitations into claim 26," and construed "integrated circuit device" to have its ordinary meaning to one of skill in the art-"a circuit constructed on a single monolithic substrate, commonly called a 'chip.' ' Id. at 1090-91 (citing *Rambus, Inc. v. Infineon Techs. AG,* No. 3:00cv524, slip op. at 70 (E.D.Va.2001)); *cf.* THE NEW IEEE STANDARD DICTIONARY OF ELECTRICAL AND ELECTRONIC TERMS 662 (5th ed.1993); IBM DICTIONARY OF COMPUTING 347 (10th ed.1994); *see also* Tex. Digital, 308 F.3d at 1202 ("unless compelled otherwise, a court will give a claim term the full range of its ordinary meaning as understood by persons skilled in the relevant art."). Even assuming that the Federal Circuit's construction is dicta, the Federal Circuit's reasoning remains applicable to the present matter, and the reasoning is persuasive. The court, as urged by Rambus, construes "integrated circuit device" as "a circuit constructed on a single monolithic substrate, commonly called a 'chip.' '

FN9. Claim 26 recites:
26. An *integrated circuit device* having at least one memory section which includes a plurality of memory cells, wherein the integrated circuit device outputs data on an external bus synchronously with respect to first and second external clock signals, the integrated circuit device comprises:

a first internal register to store a value which is representative of a number of clock cycles to transpire before the integrated circuit device responds to a read request;

delay locked loop circuitry to generate an internal clock signal using the first and second external clock signals; and

interface circuitry, coupled to the external bus to receive a read request, the interface circuitry includes a plurality of output drivers, coupled to the external bus, to output data on the external bus in response to the internal clock signal, synchronously with respect to the first and second external clock signals and in accordance with the value stored in the first internal register. U.S. Patent No. 5,954,804 (issued Sept. 21, 1999) (emph.added).

3. Synchronous Memory Device

a. Proposed constructions

Hynix argues that "synchronous memory device" should be construed to mean "a memory device in which an external clock is used for timing purposes." Rambus counters that the term should be construed as "a memory device in which address, input data and control signals are recognized and output data signals are transferred in response to an external clock." The parties agree that a "synchronous" memory device is one in which at least some operations are synchronous with respect to an external clock. *See, e.g.,* Hynix's Resp. CC Br. at 12. The parties disagree, however, over whether "synchronous" requires that all operations on the memory device be timed with respect to an external clock, or whether some operations on the memory device can be "asynchronous" while executing other operations as "synchronous." FN10

FN10. Both parties agree that "synchronized" means "having a known timing relationship with respect to." Opp. at 6 n. 2.

As noted during the tutorial, DRAM in the early 1990's were asynchronous, although not called such, until the advent of Synchronous DRAM. Thus, the development and meaning of "Synchronous DRAM" is a relatively recent phenomenon.

b. Claim language

11 of the 15 patents in suit have claims reciting the limitation "synchronous memory device." Claim 1 and asserted claim 2 of the '263 patent, for instance, recite:

1. A synchronous semiconductor memory device having at least one memory section which includes a plurality of memory cells, the memory device comprises:

a programmable register to store a value which is representative of a delay time after which the memory device responds to a read request.

2. The synchronous memory device of claim 1 further including output drivers, coupled to an external bus, to output data on the bus, in response to the read request, synchronously with respect to an external clock.

Although claiming a "synchronous memory device," nothing in the text of claim 1, upon which claim 2 depends, excludes some asynchronous operations. In addition, claim 1 does not explicitly require that address, input data and control signals be provided synchronously. Notably, claim 1 uses the term "comprises" in describing a memory device with a programmable register, thus apparently not closing the

claim to asynchronous elements. *See* Moleculon Research Corp. v. CBS, Inc., 793 F.2d 1261, 1271 (Fed.Cir.1986) ("The term 'comprising' denotes a patent claim as being 'open,' meaning that the recitation of structure in the claim is open to additional structural elements not explicitly mentioned."); M.P.E.P. s. 2173.05(h) (6th Ed.1996); *see also* '152 patent, cl. 11.

c. Ordinary meaning

Hynix offers definitions of "synchronous" from two dictionaries. Webster's Ninth New Collegiate Dictionary (2d ed.1989) defines synchronous as:

1: happening, existing, or arising at precisely the same time; 2: recurring or operating at exactly the same periods; ... 4a: having the same period; *also:* having the same period and phase.

The Oxford English Dictionary (2d ed.1989) defines synchronous as:

1.a. Existing or happening at the same time; coincident in time; belonging to the same period, or occurring at the same moment, of time; contemporary; simultaneous ...; b.... Relating to or treating of different events or things belonging to the same time or period; involving or indicating contemporaneous or simultaneous occurrence....

2.a. Recurring at the same successive instants of time; keeping time *with;* going on at the same rate and exactly together; having coincident periods, as two sets of vibrations or the like .... b. *Electr*. Applied to alternating currents having coincident periods; also to a machine or motor working in time with the alternations of current .... c. *Computer* and *Telecommunications*. Of apparatus or methods of working: making use of equally spaced pulses that govern the timing of operations....

The Authoritative Dictionary of IEEE (Institute of Electrical and Electronics Engineering) Standards Terms (5th ed. 1993) ("IEEE Dictionary") defines "synchronous" as:

A mode of transmission in which the sending and receiving terminal equipment are operating continuously at the same rate and are maintained in a desired phase relationship by an appropriate means.

Rambus offers the IEEE Dictionary (4th ed.1988) definition of "synchronous computer," a "computer in which each event or the performance of each operation, starts as a result of a signal generated by a clock." *See also* THE AUTHORITATIve Dictionary of IEEE Standards Terms 1141 (7TH ED.2000).

In contrast, the IEEE Dictionary (5th ed.1993) defines "synchronous device" more broadly, as "[a] device whose speed of operation is related to the rest of the system to which the device is connected." *See also* THE AUTHORITATIve Dictionary of IEEE Standards Terms 1141 (7TH ED.2000).

Rambus argues that "synchronous memory device" should be defined in the same way as "synchronous computer." In addition, Rambus argues that articles cited by Hynix's expert, David Taylor, all refer to DRAMs that persons of ordinary skill in the art would refer to as "asynchronous DRAMs." Murphy Reply Decl. para. 13. In contrast, the IEEE definition of "synchronous device" does not require that every operation be synchronous, but that the device's "speed of operation" be related to the rest of the system to which it is connected. Hynix also suggests that DRAMs in the late 1980's and early 1990's that timed all inputs and outputs to an external clock were more often referred to as "fully synchronous." FN11 Taylor Decl. para. 21.

FN11. The first patent issuing from the original '898 application, U .S. Pat. No. 5,319,755 ("the '755 patent"), issued on June 7, 1994.

As discussed *supra,* the Federal Circuit construed "bus" as having its ordinary meaning, and not limited to a "multiplexed bus." Here, there is no clear statement that a "synchronous memory device" must exclude asynchronous functions. Considering the changing nature of bus architecture, the scope of claims in Rambus's related SDRAM patents covering both memory devices and synchronous memory devices, and the lack of any clear statement defining "synchronous memory device" as requiring that all operations be synchronous, a broader construction of memory device than the one offered by Rambus is warranted.

d. Specification

The specification does not use or define the term "synchronous memory device." Rather, Rambus contends that numerous references in the specification imply a memory device where address, input data and control signals are required to be synchronous. The specification references that Rambus cites, however, in large part discuss a clocking scheme in the context of a multiplexed bus architecture. *See, e.g.,* '263 patent col. 8, ll. 8-32. The specification states, for instance, that "another object of this invention is to provide a method for transferring address, data and control information over a relatively narrow bus and to provide a method of bus arbitration when multiple devices seek to use the bus simultaneously." Id. at col. 3, ll. 25-29. The implication that address, data and control information must be asserted in response to an external clock, however, stems from the multiplexed bus limitation.

Although it appears that address, data and control information must be asserted in response to an external clock in order to work with the described bus architecture, nothing in the specification expressly requires it. As with the term "bus," here "[n]one of Rambus's statements constitute a clear disclaimer or disavowal of claim scope." Infineon II, 318 F.3d at 1095. Without a clear disclaimer in the specification, Rambus's attempt to narrow "synchronous memory device" based on references to a multiplexed bus in the specification is not persuasive.

e. Subsequent briefing

During the claim construction hearing, and in light of the original briefing, the court proposed the construction: "a memory device that receives an external clock to govern the response timing of the memory device's operation(s)." Hynix notes that such a construction would cover devices in which the timing of data input and output is governed by an external clock, and finds the construction acceptable. Pl.'s Supp. Memo re: "Synchronous Memory Device" and "Packet" at 2. Rambus also finds the court's tentative construction acceptable if the words "response timing" are replaced by the phrase "the timing of input and output operations" to clarify that input and output timings must both be governed by an external clock. Def.'s Supp. Memo re: "Synchronous Memory Device" and "Packet" at 1. Although the parties agree that the specification discloses a preferred embodiment in which both inputs and outputs are governed by an external clock, as discussed earlier, it appears from the claims that Rambus's construction is too narrow. The court finds that the language of the claim supports the definition of "synchronous memory device" as "a memory device that receives an external clock signal which governs the timing of the response to a transaction request."

4. Operation Code

a. Proposed constructions

The disputed term "operation code" is used in U.S. Patent Nos. 6,378,120 ("the '120 patent"), 6,378,020 ("the '020 patent"), 6,426,916 ("the '916 patent"), and 6,452,863 ("the '863 patent"). Rambus proposes that "operation code" be construed as "one or more bits to specify a type of action." Joint Claim Construction Statement ("JCCS") Ex. A at 8. Hynix submits that the term means "[b]its in a field within a packet or computer code instruction that identifies what type of action to be performed." *Id*. The dispute focuses on Hynix's attempt to limit the operation code to require that the action be performed "within a packet" or

"within a computer code instruction." Hynix further objects that Rambus's proposed construction improperly broadens the scope of what could constitute an operation code.

b. Claim language

The claims teach that there are conceptually three types of operation codes. "[T]he first operation code instructs the memory device to perform a read operation." '120 patent, cl. 1. "[T]he second operation code instructs the memory device to perform a write operation." '120 patent, cl. 2. "[T]he third operation code instructs the memory device to store the value [which is representative of a number of clock cycles of the external clock signal to transpire before the memory device outputs the data] in a programmable register on the memory device." '120 patent, cl. 12.

The dependent claims recite various properties the operation code may have. "[T]he first operation code [may] FN12 include[ ] precharge information. " '120 patent, cl. 7 (which is dependent on claim 1). "[T]he first operation code [may be] included in a request packet. " '120 patent, cl. 8 (which is dependent on claim 1). "[T]he block size information and the first operation code [may be] both included in the same request packet. " '120 patent, cl. 9 (which is dependent on claim 1). This request packet may also include address information. '120 patent, cl. 10 (which is dependent on claim 8). Finally, the operation codes are issued by a memory controller ('863 patent, cls. 1, 3) and provided to the memory device via an external bus ('120 patent, cl. 21, dependent on cl. 15).

FN12. Throughout this paragraph "may" is inserted because these are dependent claims.

Hynix argues that "operation code" should be limited to a field within a packet.FN13 The context in which the claims use "operation code" does not suggest such a limitation was intended. Claim 1 of the '120 patent (which is asserted), refers to an "operation code" that "instructs the memory device to perform a read operation." Yet, Claim 8 of the '120 patent (which is dependent on Claim 1, but not asserted) specifies that the "operation code is included in a request packet." Claim 24 of the '863 patent (which is dependent upon Claim 14, but is not asserted) also specifies "the operation code, the first block size information and address information are included in a packet." *See* '020 patent, cl. 34 (which is dependent on cl. 32).

FN13. Hynix offers no specific explanation why "operation code" should be limited to fields within a "computer code instruction." Moreover, Hynix proffers no definition for a "computer code instruction." The patents use the term "computer" inconsistently, sometimes referring to a computer as a higher level or simply different device from the present invention. Therefore, Hynix has presented no persuasive evidence demonstrating that the limitation "within a computer code instruction" applies to "operation code."

The Federal Circuit faced a similar construction issue in Infineon II. 318 F.3d at 1095. There, the court reasoned that by claiming a "bus carry[ing] device-select information without the need for separate device-select lines connected directly to individual semiconductor devices" (i.e. a bus *that is* multiplexed), Rambus showed it "did not redefine 'bus' in the specification to be a multiplexing bus." *Id*. Similarly, by specifying in certain dependent claims that the operation code is included in "a request packet," or simply "a packet," Rambus does not appear to limit "operation code" as used in other claims to bits in a field within a packet.

c. Ordinary meaning

The court looks to the relevant technical dictionaries to ascertain the ordinary and customary meaning of "operation code." Tex. Digital, 308 F.3d at 1202. The patents relevant to operation code were issued in 2001 and 2002, so the court looks to the 2001 edition of The Authoritative Dictionary of IEEE Standard Terms for guidance. "Operation code" has the following definition:

(1)(B) The code that represents or describes a specific operation. The operation code is usually the operation part of the instruction.

THE AUTHORITATIve Dictionary of IEEE Standard Terms 769 (2001 ED.).

In light of the evidence presented, the court finds this definition to be the ordinary meaning of "operation code." Rambus's proposed construction is substantially similar to this definition, and therefore comports with the ordinary meaning of "operation code." Notably, the ordinary meaning of "operation code" does not connote that it be transmitted solely within a packet.

d. Specification

To rebut the presumption that one skilled in the art would have understood "operation code" to carry its ordinary meaning, Hynix argues the specification defined the claim term by implication to include the packet limitation. *See* Bell Atl. Network Servs. v. Covad Communications Group, Inc., 262 F.3d 1258, 1271 (Fed.Cir.2001) ("when a patentee uses a claim term throughout the entire patent specification, in a manner consistent with only a single meaning, he has defined that term 'by implication" '). Hynix observes that the sole support for the meaning of "operation code" in the specification is in the AccessType field in the preferred embodiment of the request packet.

In the preferred implementation, the operation code is part of the control information. '120 patent, cl. 9, ll. 39-41. The control information is contained within two 4 bit fields that constitute the first byte of a six byte request packet. '120 patent, cl. 9, l. 25; Fig. 4. The preferred implementation labels the operation code in this packet "AccessType" ('120 patent, cl. 9, l. 35), which is depicted in Figure 4. AccessType is also depicted in additional types of packets in Figure 5 and Figure 6. The specification explains that AccessType is a field which "specifies whether the requested operation is a read or write and the type of access, for example whether it is to the control registers or other parts of the device, such as memory." '120 patent, cl. 9, ll. 43-46.

In *Toro Co. v. White Consolidated Industries, Inc.,* the Federal Circuit explained that a limitation upon a claim term may be implied from its existence in the sole preferred embodiment when "[n]o other broader concept was described as embodying the applicant's invention, or shown in any of the drawings, or presented for examination." 199 F.3d 1295, 1301 (Fed.Cir.1999). The court construed "including" and "cover" as requiring that a restriction ring be permanently attached to the cover because "[n]owhere in the specification, including its twenty-one drawings, is the cover shown without the restriction ring attached to it." *Id.* Moreover, "the specification describe[d] the advantages of the unitary structure as important to the invention." *Id.* Hynix concludes that since the sole use of "operation code" in the preferred implementation is as the AccessType field within a packet, the specification clearly implies that the construction of "operation code" should be limited to being within a packet. *See* Toro, 199 F.3d at 1301.

A weakness in Hynix's position is revealed when the preferred embodiment is viewed in light of Infineon II, 318 F.3d at 1095. The Federal Circuit held that Rambus's invention's use of a bus "is not limited to a multiplexing bus." *Id.* Stated another way, the scope of Rambus's invention includes operation on a non-multiplexed bus. The *Infineon II* court defined "multiplexing" as "the sharing of a single set of lines to send multiple types of information," such as address, data and control information. Id. at 1094. The preferred embodiment of AccessType being within a request packet is illustrated in Figure 4. The packet depicted in Figure 4 (as well as in Figures 5 and 6) requires the use of a multiplexed bus. For example, in Figure 4, the bus line carrying AccessType[0] would carry the first bit of the operation code on cycle 0, then the same bus line would carry address information on the remaining cycles. The packet depicted in Figure 6 requires the same bus line to carry control information (*i.e.,* AccessType), address information, invalid request information, and request information over the course of 12 bus cycles. The critical fact is that these packets

travel on a multiplexed bus and cannot operate on a non-multiplexed bus.

If the preferred embodiment of operation code requires the use of a multiplexed bus, but the Federal Circuit has found the invention may be operated on non-multiplexed bus, then the logical conclusion is that this cannot be the only possible embodiment of the "operation code." *See* SRI Int.'l v. Matsushita Electric Corp., 775 F.2d 1107, 1121 (Fed.Cir.1985) (the law does not require an applicant describe in the specification "every conceivable and possible future embodiment of his invention."). Consequently, Rambus's patents are distinguishable from the patents in Toro. See 199 F.3d at 1301. In implying a limitation from the preferred embodiment in *Toro,* the court found that "[t]his is not a case of limiting the claims to a 'preferred embodiment' of an invention that has been more broadly disclosed." *Id*. In contrast, here the Federal Circuit has found that a broader invention has been disclosed, one in which the claims cover operation on both multiplexed buses and non-multiplexed buses. Infineon II, 318 F.3d at 1095. Therefore, a limitation absent in the claims or ordinary meaning of "operation code" cannot be inferred from a preferred embodiment that does not describe the full scope of the claimed invention's method of operation. *See* RF Del., Inc. v. Pac. Keystone Techs., Inc., 326 F.3d 1255, 1264 (Fed.Cir.2003) (independent claims usually cover a scope broader than the preferred embodiment, especially when the dependent claims recite the precise scope of the preferred embodiment).

e. Prosecution history

Hynix's citation to Rambus's statements in the prosecution history of the '916 patent is similarly unavailing. Rambus's statements do not add any more context to the definition of "operation code" than what is disclosed in the specification.

f. Breadth

Hynix argues Rambus's definition of "operation code" improperly broadens the term to the point that "any input electrical signal with two possible voltage levels, for example, could qualify as an 'operation code' as long as some action ('on' or 'off') occurred in response." Hynix's Resp. CC Br. at 17. At first blush, this argument has some appeal. However, the claims themselves limit the practical effect of Rambus's proposed construction. For example, the theoretical input electrical signal that Hynix fears will be considered an operation code still must either "instruct the memory device to perform a read operation," ('120 patent, cl. 1), a "write operation" ('120 patent, cl. 2), or "to store the value in a programmable register on the memory device." ('120 patent, cl. 12). It must also be sampled synchronously with respect to the external clock signal. Id. Finally, it must include precharge information.FN14 However, only certain claims, like dependent claim 8 of the '120 patent, require that the operation code be contained within a request packet.

FN14. At the least the first such input signal would have to include this information.

The court is satisfied that Rambus's construction sufficiently "assign[s] a fixed, unambiguous, legally operative meaning to the claim." Liquid Dynamics Corp. v. Vaughan Co., Inc., 355 F.3d 1361, 1367 (Fed.Cir.2004). The claim language, the specification, and the prosecution history do not suggest that the patent uses "operation code" in a manner inconsistent with its ordinary meaning. Therefore, the court finds "operation code" is properly construed as "one or more bits to specify a type of action."

5. Block Size Information

a. Proposed constructions

The disputed term "block size information" is used in U.S. Patent Nos. 6,032,214 ("the '214 patent") and 6,034,918 ("the '918 patent") and the '120 and '863 patents. Rambus proposes the term be construed as "[a] value representative of a quantity of data to be transferred during a memory read or write operation." JCCS,

App. A at 11. Hynix proposes, "[i]nformation that specifies the total amount of data that is to be transferred on the bus in response to a [transaction] request." *Id*. The dispute focuses on the amount of data to which the term refers.

b. Claim language

"In Rambus's invention, the user can specify the amount of data to be transferred over the bus during a bus transaction. This value is represented by the term 'block size [information].' ' Infineon I, 2001 WL 34138091 at *16. The claims state that "first block size information defines a first amount of data to be output by the memory device onto a bus in response to a read request." '918 patent, cl. 18. The memory device receives the first block size information and responds by "outputting the first amount of data corresponding to the first block size information." Id. Similarly, second block size information typically corresponds to the amount of data to be input in response to a second transaction request. '918 patent, cl. 3.

c. Interpretation

Rambus's first objection to Hynix's proposed construction is that it can be interpreted as requiring the value of "block size information" to be equal to the amount of data to be transferred. If this were the case, for example, then when a request called for 1024 bits of data, the value that conveyed block size information would also have to be 1024. Hynix has allayed these fears by pointing out that "the term 'specify' [in its proposed construction] only indicates that the 'block size information' is a code that represents the total size of the block of data to be transferred." Hynix at 20; *see also* Reply at 8 n. 2. Hynix also notes that "Rambus's construction is ambiguous in failing to specify that the 'block size information' defines a single block of data to be transferred in a single device access. Hynix's proposed construction does not contain this ambiguity and is consistent with the specification." Opp. at 19.

The court finds that block size information must be a value that corresponds to the total number of bits to be transferred. Such a construction comports with the construction of the term by the Eastern District of Virginia and is supported by the claims and the specification. Infineon I, 2001 WL 34138091 at *17 (construing "block size" as "information that specifies the total amount of data that is to be transferred on the bus in response to a transaction request").

Rambus also seeks to clarify in its reply brief that the "total amount" referred to in "block size information" is the data to be transferred from a single device, not from every memory device in a system. Despite Rambus's fear, nothing in the claims, the specification, or Hynix's arguments suggests that "block size information" relates to the amount of data to be transferred from every memory device in a system. Thus, although the court agrees that the intrinsic evidence supports the position that "block size information" relates only to the amount of data to be transferred from a single device, the court does not agree that Hynix's proposed construction is susceptible to the interpretation that "block size information" refers to the amount of data to be transferred from every memory device in a system. "Block size information" is construed as "information that specifies the total amount of data that is to be transferred on the bus in response to a transaction request."

6. Precharge Information

a. Proposed constructions

The disputed term "precharge information" is used in the '120 and '916 patents. Hynix proposes that "precharge information" be construed as "[i]nformation denoting whether a memory array (or portion of a memory array) should be precharged." JCCS, Ex. A at 13. Rambus proposes a "value that is related to an establishment of a pre-defined voltage state." *Id*.

Originally, Rambus challenged Hynix's definition on the grounds that precharging relates to the sense amps,

which would be excluded from Hynix's definition because the sense amps are not part of the memory array. At the hearing, Hynix agreed that "memory array" could be replaced in their proposed construction with "sense amplifiers and bit lines." Tr. 106:1-7. Therefore, Hynix's amended construction of precharge information is "information denoting whether the sense amplifiers and/or bit lines (or a portion of the sense amplifiers and/or bit lines) should be precharged." Tr. 104:22-24.FN15 In light of Hynix's amendment, the only dispute is whether precharge information is simply "related to [the] establishment of a pre-defined voltage state" or more specifically denotes whether the sense amps and bitlines "should be precharged."

FN15. Hynix uses the "or" construction.

Hynix objects that Rambus's proposed construction of precharge information is devoid of meaning or connection to the use of precharging in the memory device. This objection is well taken. Construing "precharge information" as simply "a value that is related to an establishment of a pre-defined voltage state" imparts no meaningful guidance as to what the term means. Bell Atl., 262 F.3d at 1270 ("ordinary meaning of the non-technical term 'mode' is sufficiently broad and amorphous that the scope of the claim can be reconciled only with recourse to the written description").

b. Claim language

Before or after each read or write operation at a new address, two components of a DRAM must be precharged, "the bitlines in the [memory] array and the sense amplifiers." Taylor Decl. para. 87; *see also* JCCS, Ex. F (JOHN Y. CHEN, CMOS DEVICES AND TECHNOLOGY FOR VLSI 115 (1990)). All of the asserted claims containing the precharge information limitation, in both patents, are identical. They state:

The method of claim 1 wherein the first operation code includes precharge information.FN16

FN16. In all cases, the claim containing "precharge information" is a dependent claim. In the '120 patent claim 7 contains the limitation and is dependent on claim 1. In the '120 patent claim 33 contains "precharge information" and is dependent upon claim 29. In the '916 patent claim 9 contains the limitation and is dependent upon claim 1.

This claim language by itself does not provide clear meaning. It does, however, provide an important contextual backdrop. The plain meaning of the term shows it must convey information related to precharging. The claim teaches that the precharge information is included in the first operation code, which means the information is conveyed as part of a command. This implies the precharge information is connected to instructing the device (or a portion of the device) to perform an action. *See supra* (construction of operation code).

c. Specification

Rambus's proposed construction does not include a connection between the act of precharging and a specific component of the memory device. The context in which "precharge" is used in the specification consistently implies such a connection is necessary. Each time the specification discusses precharging it is in connection with a component of the device. More importantly, the specification teaches the precharge information contained in the operation code is used to determine the access mode. The access mode, in turn, "determines whether the DRAM should precharge the sense amplifiers or should save the contents of the sense amps for a subsequent page mode access." '263 patent, cl. 10, ll. 8-14.

Thus, the precharge information does not simply convey a value representing the establishment of a pre-defined voltage state. Instead it conveys whether the device should precharge the "sense amps (and hence

the bit lines)" ('263 patent, cl. 10, l. 43), or not precharge the sense amps so that they can retain the data to be sensed on the next read ('263 patent, cl. 10, ll. 25-30). The parties do not dispute what the specification means by "precharge." Therefore, the court finds that the specification implies "precharge information" as information relating specifically to whether or not a component of the device should be precharged.FN17 Rambus's definition does not contain this necessary connection between precharging and specific components of the device. Consequently, "precharge information" is construed as "information denoting whether the sense amplifiers and/or bit lines (or a portion of the sense amplifiers and/or bit lines) should be precharged."

FN17. As discussed, the parties have agreed that the this component of the device is actually the sense amps and/or the bit lines.

7. Access Time/ Access Time Register/ Delay Time

a. Proposed constructions

To optimize transmissions over the bus, the invention attempts to coordinate individual DRAM outputs by injecting a certain time delay before each device responds to a request. A value representing the amount of time the device is to delay is stored in one or more access time registers on each device.

Rambus and Hynix dispute the construction of three related terms: (1) access time register; (2) access time; and (3) delay time. These terms are conceptually interrelated which requires they be construed jointly. "Access time register" is used in '214 patent, claim 18 and the '918 patent, claim 24. The parties have agreed to the construction of "register" as "a data storage element or group of data storage elements not part of a memory array that can store one or more bits of information." Rambus proposes "access time register" be construed as "[a] data storage element to store a value representative of an access time delay." Hynix proposes it be construed as "[a] register programmable to store information representing a particular access time." JCCS, Ex. A at 24.

"Access time" is used throughout the patents yet never as a separate term in the asserted claims. Hynix argues the term should be separately construed by the court because the parties have agreed to a construction of "register," and because both parties use the term in their proposed constructions of several other terms. Hynix proposes "access time" be construed as "[t]he time between the initiation of a memory access and the availability of data at the outputs." JCCS, Ex. A at 22. Rambus opposes a construction of "access time" because the term is only used within the asserted claims as part of "access time register." Although Rambus's briefing contains several arguments in opposition to Hynix's proposed definition, Rambus does not provide a proposed construction for "access time." JCCS, Ex. A at 22.

"Delay time" is used in the '263, '918, '365, and '195 patents. Hynix proposes the term be construed as "[t]he time between the initiation of a memory access and the availability of data at the outputs." JCCS, Ex. A at 25. Rambus proposes "[a]n amount of time before commencing a subsequent action." Id.

b. Access Time Register

i. Claim Language

Two asserted claims use the term "access time register." Each provides significant context for construing the term. Claim 18 of the '214 patent states:

The method of claim 15 [describing the read and output of data synchronously with respect to a first and second external clock signal] further including storing a code in an access time register, the code being representative of a number of clock cycles of the first and second external clock signals to transpire before

data is output onto the bus in response to the first read request, wherein the first amount of data corresponding to the first block size information is output after the number of clock cycles transpire.

Claim 24 of the '918 patent states:

The method of claim 18 [describing the read and output of data synchronously with respect to the external clock signal] further including storing a delay time code in an access time register, the delay time code being representative of a number of clock cycles to transpire before data is output onto the bus after receipt of a read request and wherein the first amount of data corresponding to the first block size information is output in accordance with the delay time code.

Throughout the patents-in-suit various phrases are used to describe what the value in the "access time register" is meant to represent. Hynix offers "a particular access time." Rambus offers "an access time delay." For puposes of this subsection, in an effort to avoid confusion, the court will use the term "delay time code." FN18

FN18. This is not to be interpreted interchangeably with the disputed term "delay time."

ii. Ordinary meaning

Hynix argues that the contents of the access time register should be defined as a value representing a time equivalent to the ordinary meaning of "access time." The ordinary meaning of "access time" is "the time interval between the instant at which data are called for from a storage device and the instant delivery is completed, that is, the read time." THE AUTHORITATIve Dictionary of IEEE Standards Terms 7 (7TH ED.2001). HYNIX'S PROPOSED CONSTRUCTION OF "ACCESS TIME" IS SUBSTANTIALLY SIMILAR TO ITS ORDINARY MEANING..

Rambus contends that the claims asserted use the term "access time" as simply a label for that type of register. The label, according to Rambus, does not thereby define the contents of the register. The claims' explicit statement that the access time register stores a delay time code supports Rambus's argument. Delay time, as discussed below, is not necessarily equal to Hynix's construction of "access time." Therefore, the ordinary meaning of the label "access time register" does not control the construction of its contents.

iii. Specification

Hynix seeks to limit the delay time code to "a particular access time." Hynix further seeks to precisely define how such "access time" is measured. JCCS, Ex. A at 22. Rambus argues the claims should not be limited to registers where the delay time (represented by the delay time code) is equal to the access time as measured by Hynix.

Hynix's construction of "access time" appears to describe the physically minimum access time. As Rambus observes, in one sense, "access time" describes a physical characteristic of the memory device. It is the minimum amount of time in which it is physically possible for a device to receive a request and then complete its response, whether that response be to write a block of data or to output a block of data through the output pins. *See* THE AUTHORITATIve Dictionary of IEEE Standards Terms 7 (7TH ED.2001). AS NOTED DURING THE TUTORIAL, THE PHYSICAL ACCESS TIME OF A DEVICE IS TYPICALLY A FIXED CONSTANT, PREDETERMINED BY THE ACCESS MODE, THE PHYSICS OF THE CHIP, AND THE INTERACTION WITH EXTERNAL VARIABLES SUCH AS TEMPERATUREE OR VOLTAGE.

First, in a preferred embodiment, the specification teaches:

The value stored in a slave access-time register 173 is preferably one-half the number of bus cycles for which the slave device should wait before using the bus in response to a request.

'263 patent, cl. 15, ll. 57-60. As this passage illustrates, the access time register changes the amount of time in which a memory device returns data depending on the value stored in the register. Murphy Reply Decl. para. 25. The critical technical aspect of this concept, that is not necessarily included in Hynix's proposed construction of "access time," is the injection of a potential and variable delay in the device's response.

Second, the specification reveals that it would be improper to limit the delay time, or the value stored in the access time register, to any single value. The specification states:

The configuration master should choose and set an access time in each access-time register 173 in each slave to a period sufficiently long to allow the slave to perform an actual, desired memory access. For example, for a normal DRAM access, this time must be longer than the row address strobe (RAS) access time. If this condition is not met, the slave may not deliver the correct data. The value stored in a slave access-time register 173 is preferably one-half the number of bus cycles for which the slave device should wait before using the bus in response to a request. Thus an access time value of '1' would indicate that the slave should not access the bus until at least two cycles after the last byte of the request packet has been received. The value of AccessReg0 is preferably fixed at 8 (cycles) to facilitate access to control registers. '263 patent, cl. 15, ll. 51-65.

Thus, the patent contemplates that the user can set the delay time to any desired value. The preferred embodiment takes steps to teach what the patentee believed to be the optimal delay times for the various access modes. However, the consistent use of terms such as "should," "preferably," and "choose" demonstrates the user is not required to set the delay time to any fixed or pre-determined value. Therefore, this court will not read such a limitation from the preferred embodiment into the construction of "access time register."

Similarly, it would be improper to limit the measurement of the delay time to ending at any specific pre-defined event. The specification explains:

[A] slave should preferably respond to a request in a specified time, sufficient to allow the slave to begin *or* possibly complete a device-internal phase including any internal actions that must precede the subsequent bus access phase.

'263 patent, cl. 8, ll. 39-42 (emph.added).

This passage demonstrates the patent contemplates the possibility that the delay time could be set to end either before or after the completion of a device internal phase. Rambus, however, agreed at the hearing that the time can be limited to commencing when the device receives a transaction request. Tr. 118:21.FN19

FN19. In the construction of "access time register" the court adopts below, the court uses the phrase "receiving a transaction request" to describe the starting point of this time delay. To the extent this phrase contains any ambiguity, the court notes that the claims using "access time register" often describe the starting and ending events used to measure this delay time code. The court intends for its construction to be interpreted as a generic term which is further defined by the specific claims at issue. Tr. 117:2-118:4.

iv. Rambus's construction is ambiguous

Rambus proposes the value in the access time register be construed as representing "access time delay."

JCCS, Ex. A at 24. Hynix objects that this construction is circular and ambiguous. Notably, Rambus made similar objections to Hynix's proposed construction of "access time." Those same objections undermine the soundness of using "access time delay" in the construction. Having found that the ordinary meaning of "access time" does not necessarily equal the delay time, the court finds "access time delay" provides little guidance when evaluating possible infringement.

In searching for a clearer way to define the value stored in the access time register, the court finds the specification's description to be accurate and clear. Therefore, "access time register" is construed as "a data storage element to store a value representative of a time a device must wait from receiving a transaction request before responding to a transaction request." Tr. 118:18-20.

c. Delay Time

Hynix proposes "delay time" be construed using the same definition it proposed for "access time." For the reasons discussed in reference to the "access time register," "delay time" cannot be limited to equaling any fixed access time, nor can it be precisely measured in the fashion Hynix proposes. In addition, Hynix includes in its definition of delay time, "the availability of data at the outputs." Yet, the claims using "delay time" separately already set forth the action that occurs after the delay time expires. For example, claim 1 of the '263 patent involves "a programmable register to store a value which is representative of a delay time after which the memory *responds to a read request*." (emphasis added) Adopting Hynix's construction of delay time would render the representative claim 1's expression of the subsequent action (emphasized in quotation) superfluous.

Since each claim in which "delay time" is used as a separate term (as opposed to "delay time code") provides sufficient context to ascertain the purpose and functionality of the concept, "delay time" shall simply be construed "as an amount of time that must transpire before commencing an action." The court finds this construction to comply most closely with the term's ordinary meaning. *See* OXFORD ENGLISH DICTIONARY (2d ed.1989).

8. "Value That is Representative of an Amount of Time to Transpire"/"Value Which is Representative of a Delay Time"/"Value Which is (or Code Being) Representative (or Indicative) of a (Preprogrammed) Number of Clock Cycles"

The parties dispute the following three terms: (1) "value that is representative of amount of time to transpire" used in the '916 patent; (2) "value which is representative of a delay time" used in the '263, '365, and '195 patents; (3) "value which is (or code being) representative (or indicative) of a (preprogrammed) number of clock cycles" used in the '263, '443, '214, '918, '195, '592, '152, '120, and '916 patents. Hynix proposes each of these terms be defined as "[i]nformation representing a particular access time." JCCS, Ex. A at 26-28. Rambus contends the terms are self-explanatory in light of their context within the claims. Rambus is correct. The court finds the patents used these terms in a manner equivalent to delay time code or "delay time." The problems discussed with Hynix's proposed construction of "access time register" and "delay time" apply equally to its construction of these terms.

Accordingly, the court adopts Rambus's proposed construction for each of these terms. Each term is interpreted to represent a value conceptually similar to the delay time code and "delay time" discussed above. "Value that is representative of amount of time to transpire" is construed as "[i]nformation that indicates an amount of time which is to occur." JCCS, Ex. A at 26. "Value which is representative of a delay time" is construed as "information which indicates a delay time." *Id*. "Value which is (or code being) representative (or indicative) of a (preprogrammed) number of clock cycles" is construed as "information which indicates a number of clock cycles."

9. Data

In light of the court's refusal to construe "device" as requiring a multiplexed bus, the parties agree that construction of "data" is no longer necessary. (Tr. 107:10-108:11.).

10. Control Information

Since the court does not construe "device" as requiring a multiplexed bus, the parties agree that construction of "control information" is no longer necessary. (Tr. 107:10-108:11.)

11. "First External Clock" and "Second External Clock"

a. Proposed constructions

Hynix contends that "first external clock" should be construed as "a periodic signal received by the memory device from an external source to provide first timing information." *See* Infineon I, 2001 WL 34138091 at *26. Rambus proposes that the term should be construed the same as "external clock signal"-"a periodic signal from a source external to the device to provide timing information."

Similarly, Hynix contends that "second external clock" should mean "a periodic signal received by the memory device from an external source to provide second timing information that is different from the first timing information." *See* Infineon I, 2001 WL 34138091 at *26. Rambus, in contrast, proposes second external clock signal to be interpreted as "another external clock signal."

The parties agree that "external clock signal" should be construed as "a periodic signal from a source external to the device to provide timing information." JCCS at 3. They disagree over whether the terms "first" and "second" refer to timing, or whether they refer to two separate signals without reference to time. "Although referred to as a 'clock' by one skilled in the art, the clock of a memory chip is actually a set of timing information derived from an oscillating reference voltage ("VREF") which cycles between two voltage levels." Infineon I, 2001 WL 34138091 at *24. As Rambus claimed in *Infineon I,* Rambus's proposed definitions here "do not require that the two signals contain different timing information," while Hynix's construction requires "that the second signal contain different information from the first." *Id*.

In a July 28, 2003 order, this court vacated in its entirety its previous November 21, 2001 order granting partial summary judgment to Hynix finding, *inter alia,* that "the elements of collateral estoppel are no longer met in this case." Order of 7/25/03 at 3. Besides briefing the collateral estoppel issue extensively, Rambus offers in support of its construction the IEEE Dictionary definitions for "clock" and "signal." *See* JCCS at 17.

To operate the Rambus bus architecture at high speed, "[e]very system, every ... chip, every component on the bus has to be operating under the exact same timing constraints. That's why it's important and valuable ... to use a clock design that will synchronize everything together." Infineon I, 2001 WL at 34138091 at n. 38. Reviewing figures 8A and 8B of the '918 patent, FN20 the court first explained that chips N and O were located in different positions along the bus lines, and therefore received the "clock signals at different points in time due to their locations relative to the origin of the clock signal." Id. at *25. In order to correct this delay, the memory system reflects a signal along a second line to create a second clock signal, and from these two signals "chips N and O create an internal clock signal which corrects the clock skew caused by propagation delay." Id. Notably, Rambus's expert in *Infineon* admitted that in order to correct the skew, the two signals must contain different information. *Id*. The district court went on to note that the only embodiment of the clock in the entire specification required two external signals containing different information in order to create an internal clock, thus correcting the clock skew problem. *See id*. at *26.

FN20. U.S. Patent No. 6,034,918. These figures are the same for the '152 and '263 patents.

Besides introducing evidence from the IEEE Dictionary defining the terms "clock" and "signal," Rambus does not address the *Infineon* district court's analysis. Rambus also fails to suggest an alternative embodiment in the specification under its proposed construction that would address the clock skew problem. "Where the specification makes clear that the invention does not include a particular feature, that feature is deemed to be outside the reach of the claims of the patent, even though the language of the claims, read without reference to the specification, might be considered broad enough to encompass the feature in question." Scimed Life Sys. v. Adv. Cardiovascular Sys., 242 F.3d 1337, 1341 (Fed.Cir.2001); Watts v. XL Sys., Inc., 232 F.3d 877, 883 (Fed.Cir.2000) (where specification describes only one method to achieve sealing connection, claim limited to that disclosed method); Toro Co. v. White Consol. Indus., 199 F.3d 1295, 1301 (Fed.Cir.1999) (limiting claims to preferred embodiment, and noting the "specification shows only a structure whereby the restriction ring is 'part of' the cover, in permanent attachment. This is not simply the preferred embodiment; it is the only embodiment.").

The court construes "first external clock" as "a periodic signal received by the memory device from an external source to provide first timing information," and "second external clock" as "a periodic signal received by the memory device from an external source to provide second timing information that is different from the first timing information."

III. CLAIM CONSTRUCTION

Having considered the papers submitted by the parties and the arguments of counsel during the claim construction hearing, the court interprets the disputed claim terms as set forth below. The disputed claim terms are identified in bold.

CLAIM LANGUAGE	CONSTRUCTION
device	no separate construction
integrated circuit device	a circuit constructed on a single monolithic
	substrate, commonly called a 'chip'
synchronous memory device	a memory device that receives an external clock
	signal which governs the timing of the response to
	a transaction request
operation code	one or more bits to specify a type of action
block size information	information that specifies the total amount of data
	that is to be transferred on the bus in response to a
	transaction request
precharge information	information denoting whether the sense amplifiers
	and/or bit lines (or a portion of the sense amplifiers
	and/or bit lines) should be precharged
data	no construction
control information	no construction
synchronized	having a known timing relationship with respect to

first external clock	a periodic signal received by the memory device from an external source to provide first timing information
second external clock	a periodic signal received by the memory device from an external source to provide second timing information that is different from the first timing information
access time	no separate construction
access time register	a data storage element to store a value representative of a time a device must wait from receiving a transaction request before responding to a transaction request
delay time	an amount of time that must transpire before commencing an action
value that is representative of an amount of time to transpire	information that indicates an amount of time which is to occur
value which is representative of a delay time	information which indicates a delay time
value which is (or code being) representative (or indicative) of a (preprogrammed) number of clock cycles	information which indicates a number of clock cycles
request to provide data	a series of bits used to request a read of data from a memory device where the request identifies what type of read to perform

III. ORDER

For the foregoing reasons, IT IS SO ORDERED.

N.D.Cal.,2004.
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