United States District Court,
E.D. Texas, Beaumont Division.

MOTOROLA, INC,
v.
ANALOG DEVICES, INC.

No. 1:03-CV-131

June 7, 2004.

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MEMORANDUM OPINION AND ORDER CONSTRUING CERTAIN CLAIMS OF UNITED STATES PATENT NO. 5,896,543 **(GARDE), NO. 5,175,550 (KATTMANN), NO. 6,289,300 B1 (BRANNICK), NO. 6,230,119 BL (MITCHELL), AND NO. 4,758,945 (REMEDI)**

RON CLARK**, District Judge.**

Plaintiff, Motorola, Inc. ("Motorola"), filed suit claiming infringement of five patents by Analog Devices, Inc. ("A.D.I."). A.D.I. counter-claimed alleging infringement by Motorola of six other patents. All of the patents involve various aspects of microchip production, manufacture, programming, or design. The court conducted a hearing for the purpose of hearing evidence and argument to assist the court in interpreting the meaning of certain disputed claims of 11 different patents. This order will construe the disputed claims of United States Patent No. 5,896,543 ("the Garde patent"), United States Patent No. 5,175,550 ("the Kattmann patent"), United States Patent No. 6,289,300 Bl ("the Brannick patent"), United States Patent No. 6,230,119 Bl ("the Mitchell patent"), and United States Patent No. 4,758,945 ("the Remedi patent"). Having carefully considered the parties' briefs, the testimony, and exhibits admitted into evidence, the referenced patents, and the arguments of counsel, the court now makes the following findings and construes the disputed terms as follows.

STANDARD FOR CONSTRUING CLAIM TERMS

In Markman v. Westview Instruments, Inc., 52 F.3d 967 (Fed.Cir.1995) ("*Markman I*"), the Federal Circuit held that claim construction is a matter of law. In affirming this decision, the Supreme Court in Markman v. Westview Instruments, Inc., 517 U.S. 370, 116 S.Ct. 1384, 134 L.Ed.2d 577 (1996) ("*Markman II*"), stated, "[W]e hold that the construction of a patent, including terms of art within its claims, is exclusively within the province of the court," Id. at 1387, and "... judges, not juries, are the better suited to find the acquired meaning of patent terms." Id. at 1395.

The duty of the trial judge is to determine the meaning of the claims at issue, and to instruct the jury accordingly. In the exercise of that duty, the trial judge has an independent obligation to determine the meaning of the claims, notwithstanding the views asserted by the adversary parties, (citations omitted)

Exxon Chemical Patents, Inc. v. Lubrizoil Corp., 64 F.3d 1553, 1555 (Fed.Cir.1995).

In performing this duty, this court is guided by several principles. The claims should be construed in light of the ordinary meaning of the claim language, as well as the patent specification and prosecution history. Markman I, 52 F.3d at 979-80; *see alsoVitronics* Corp. v. Conceptronic, Inc. 90 F.3d 1576, 1582 (Fed.Cir.1996).

The court should first determine the ordinary meaning of a disputed term. There is a "heavy presumption" that the terms used in claims "mean what they say and have the ordinary meaning that would be attributed to those words by persons skilled in the relevant art." Tex. Digital Sys., Inc. v. Telegenix, Inc., 308 F.3d 1193 (Fed.Cir.2002).

It is well established that courts are to determine the plain, ordinary meaning of a claim term *before* turning to the specification. As the Federal Circuit has stated:

... consulting the written description and prosecution history as a threshold step in the claim construction process, *before* any effort is made to discern the ordinary and customer meanings attributed to the words themselves, invites a violation of our precedent counseling against importing limitations into the claims." Tex. Digital, 308 F.3d at 1204 (emphasis supplied).

It is entirely appropriate for a court to look to dictionaries to determine the plain and ordinary meaning of a disputed claim term. *Id*. at 1202.

A dictionary is not prohibited extrinsic evidence, and is an available resource of claim construction. Although a dictionary definition may not enlarge the scope of a term when the specification and the prosecution history show that the inventor, or recognized usage in the field of the invention, have given the term a limited or specialized meaning, a dictionary is often useful to aid the court in determining the correct meaning to be ascribed to a term as it was used.

Vanguard Products Corp. v. Parker Hannifin Corp., 234 F.3d 1370, 1372 (Fed.Cir.2000).

Then, the court should look to the intrinsic evidence of record, that is, the patent specification, and, if in evidence, the prosecution history, to determine whether the patentee clearly intended a meaning different from the ordinary meaning or whether he clearly disavowed the ordinary meaning in favor of some special meaning. *See* Markman I, 52 F.3d at 979.

Claim terms take on their ordinary and accustomed meanings unless the patentee demonstrated a "clear intent" to deviate from the ordinary and accustomed meaning of a claim term by redefining the term in the patent specification. Johnson Worldwide Assoc., Inc. v. Zebco Corp., 175 F.3d 985 (Fed.Cir.1999).

Claims must be read in view of the specification, of which they are a part. Autogiro 384 F.2d at 397, 155 USPQ at 702; *see* Winans v. Denmead, 56 U.S. (15 How.) at 338; *Bates v. Coe,* 98 U.S. at 38-39. The specification contains a written description of the invention that must enable one of ordinary skill in the art to make and use the invention. For claim construction purposes, the description may act as a sort of dictionary, which explains the invention and may define terms used in the claims.

Markman I, 52 F.3d at 979.

The Federal Circuit offered guidance on how the written description can be helpful in determining the meaning of claims in Scimed Life Systems v. Advanced Cardiovascular, 242 F.3d 1337 (Fed.Cir.2001).

While it is true, of course, that "the claims define the scope of the right to exclude" and that "the claim construction inquiry, therefore, begins and ends in all cases with the actual words of the claim," Renishaw PLC, 158 F.3d at 1248, 48 USPQ 2d at 1121, the written description can provide guidance as to the meaning of the claims, thereby dictating the manner in which the claims are to be construed, even if the guidance is not provided in explicit definitional format.

The patentee may also deviate from the plain and ordinary meaning by characterizing the invention in the prosecution history using words or expressions of manifest exclusion or restriction, representing a "clear disavowal" of claim scope. Teleflex, Inc. v. Ficosa N. Am. Corp., 299 F.3d 1313, 1327 (Fed.Cir.2002). However, absent a "clear indication" from the patent specification or a "clear disavowal" in the prosecution history, there is a "heavy presumption" that a claim term is given its plain and ordinary meaning. Tex. Digital, 308 F.3d at 1202.

Extrinsic evidence may be considered if needed to assist in determining the meaning or scope of technical terms in the specification or claims to one of ordinary skill in the art. *Vitronics* at 1583.

THE GARDE PATENT

United States Patent No. 5,896,543**,** the **Garde** patent, is held by A.D.I., and was issued on April 20, 1999. The Garde patent relates to the field of digital signal processors (DSPs). DSPs are typically used in "real-time" applications, and those applications tend to be intensive in memory access operations and require the input and output of large quantities of data. The Garde patent seeks to enhance the performance of DSPs by using two computational units in parallel, with the two computational units sharing a common memory. Instructions and operands that are fetched from the shared memory may be sent to one of the two computational units for processing. Each of the computational blocks includes a register file, an arithmetic/logic unit (ALU), and a multiplier. Claims 1, 3 and 20-23 are asserted in this case.

Disputed Claim Terms of the Garde Patent

The disputed claims are copied below with each disputed claim term printed in bold type.

1. A **digital signal processor** comprising:

a memory for storing **instructions** and operands for **digital signal computations;** a **core processor connected** to said memory, said core processor compromising; a **program sequencer** for generating instruction addresses for fetching selected ones of said instructions from said memory; a first computation block for performing a first subset of said digital signal computations **under control of** said program sequencer using a **first subset of said instructions** and a first subset of said operands; and a second computation block for performing a second subset of said digital signal computations under control of said program sequencer using a **second subset of said instructions** and a second subset of said operands, said first and second computation blocks each comprising a **register file** for temporary storage of operands and results, a **multiplier** for performing multiplication operations, an ALU for performing arithmetic operations and a shifter for performing shifting operations; and **means for transferring said first subset of said instructions and said first subset of said operands from said memory to said first computation block for execution and for transferring said second subset of said instructions and said second subset of said operands from said memory to said second computation block for execution,** wherein said first and second computation blocks share said memory.

3. A **digital signal processor** as defined in claim 1 wherein said **multiplier** includes **means for selectably executing** 32-bit by 32-bit multiplication instructions or quad 16-bit by 16-bit multiplication instructions.

20. A **digital signal processor** as defined in claim 1 wherein said means for transferring includes **means for transferring said instructions and operands from said memory to one or both of said first and second computation blocks during each clock cycle.**

21. A digital signal processor as defined in claim 1 wherein said **first and second subsets of said instructions are the same.**

22. A **digital signal processor** as defined in claim 1 wherein said **first and second subsets of said instructions are different.**

23. A method for **digital signal processing** comprising the steps of: storing instructions and operands for **digital signal computations** in memory; in a **program sequencer,** generating instruction addresses for fetching selected ones of the instruction from the memory; in a first computation block comprising a register file for temporary storage of operands and results, a multiplier for performing multiplication operations, an ALU for performing arithmetic operations and a shifter for performing shifting operations, performing a first subset of the digital signal computations **under control of** the program sequencer using a **first subset of the instructions** and a first subset of the operands; in a second computation block comprising a **register file** for temporary storage of operands and results, a **multiplier** for performing multiplication operations, an **ALU** for performing arithmetic operations and a shifter for performing shifting operations, performing a second subset of the digital signal computations under control of the program sequencer using a **second subset of the instructions** and a second subset of the operands; and **transferring the first subset of the instructions and the first subset of the operands from the memory to the first computation block for execution and transferring the second subset of the instructions and the second subset of the operands from the memory to the second computation block for execution,** wherein said first and second computation blocks share said memory. **"digital signal processor"-claims 1, 3, 20-22**

This phrase is found in claims 1, 3 and 20-22. Initially, ADI proposed that the term be construed to mean "a processor specifically designed for implementing digital signal filters (*e.g.,* FFT) for data processing, *e.g.,* audio or image data, in real-time." Motorola first proposed the term be defined as "a special purpose

computer that is designed to optimize performance for digital signal processing applications, such as, for example, fast Fourier transforms, digital filters, image processing and speech recognition." In a letter dated January 28, 2004, Motorola proposed a slightly modified construction, proposing that "digital signal processor" be defined to mean "a special purpose computer that is designed to optimize performance for at least one of a set of applications, such as, for example, fast Fourier transforms, frequency filtering, image processing and speech recognition," citing Garde patent, 1:11-16. By letter dated February 6, 2204, ADI responded by offering its own modified construction, proposing "a special purpose digital computer designed to perform, in real-time, highly numeric computations for applications such as fast Fourier transforms, digital filters, image processing and speech recognition." ADI relies on the first paragraph under the "Background" section in the Garde patent specification, as well as on certain information from Motorola's website. ADI also relies on definitions taken from McGraw-Hill Dictionary of Scientific and Technical Terms (5th ed., 1994) for the words "signal," "signal processing" and "digital." Motorola relies specifically on the first sentence in the "Background" section of the Garde patent specification. Central to the dispute between the parties is whether a "real-time" requirement should be included within the interpretation of this term.

The dictionary definitions provided by ADI are not helpful in reaching the construction proposed by ADI. In particular, none of those definitions require that the processing of data be in real-time. The specification of the Garde patent expressly defines a "digital signal computer, or digital signal processor" to be "a special purpose computer that is designed to optimize performance for digital signal processing applications, such as, for example, fast Fourier transforms, digital filters, image processing and speech recognition." Garde patent, 1:12-16. While the specification does state that DSP applications "are typically characterized by real-time operation, high interrupt rates and intensive numeric computations," it does not indicate that these applications are necessary characteristics of DSPs, nor does it indicate that these applications, in and of themselves, define a DSP.

Motorola's modified proposed construction for the term "digital signal processor" is very similar to that taken from the patent specification. ADI's modified proposed construction for "digital signal processor" is similar to Motorola's modified proposal, except that ADI continues to propose that the definition include a "real-time" requirement. Again, the patent specification does not support a requirement that the "digital signal processor" perform operations "in real-time," saying only that "digital signal processor applications are *typically* characterized by real-time operation, high interrupt rates and intensive numeric computations." Garde patent, 1:17-19.

The use of the term "digital signal processor" throughout the Garde specification is consistent with the definition given by the Applicant and set out in the specification. Therefore, the Court interprets this claim phrase in claims 1,3, and 20-22 as follows:

"digital signal processor" means: a special purpose computer that is designed to optimize performance for digital signal processing applications, such as, for example, fast Fourier transforms, digital filters, image processing and speech recognition.

"digital signal processor"-claim 23

This phrase is found in the preamble of claim 23 of the Garde patent. ADI proposes that the phrase should mean "processing audio or image data by implementing digital signal filters (*e.g.,* FFT) in real-time." ADI again points to a portion of the patent specification, as well as to the Motorola website and to three

definitions from the McGraw-Hill Dictionary of Scientific and Technical Terms (5th ed., 1994). Motorola proposes that the phrase should mean "a method by which a digital signal processor optimizes performance for digital signal processing applications, such as, for example, fast Fourier transforms, digital filters, image processing and speech recognition," again citing from the "Background" section of the Garde patent specification.

In its January 28, 2004 letter, Motorola offered a slightly modified construction for the term "digital signal processing," offering the definition of "a method in which a special purpose computer optimizes performance for at least one of a set of applications, such as, for example, fast Fourier transforms, frequency filtering, image processing and speech recognition," again citing Garde patent, 1:11-16. In its February 6, 2004 letter, ADI offered a modified proposed construction of "real-time performance on a special purpose digital computer of highly numeric computations for applications such as fast Fourier transforms, digital filters, image processing and speech recognition," citing the Garde patent, 1:11-21.

ADI relies on the 1994 edition of the McGraw-Hill Dictionary of Scientific and Technical Terms, which defines "signal processing" to mean "extraction of information from complex signals in the presence of noise, generally by conversion of signals into digital form followed by analysis using various algorithms." ADI also relies on that same source to define "digital" to mean "pertaining to data in the form of digits." From these definitions, "digital signal processing" would refer to the extraction of information from digital signals in the presence of noise, followed by analysis using various algorithms.

Motorola's modified proposed construction is basically a restatement of its proposed definition for the term "digital signal processor." ADI, on the other hand, continues to propose a "real-time" requirement, but otherwise defines "digital signal processing" to mean "performance ... of highly numeric computations...." The specification does indicate that "[d]igital signal processing applications are typically characterized by real-time operation, high interrupt rates and intensive numeric computations." Examples of digital signal processing applications given in the patent are fast Fourier transforms, digital filters, image processing and speech recognition. Garde patent, 1:12-19. These characteristics and examples appear to fall within the general meaning of "digital signal processing" as gleaned from the 1994 McGraw-Hill Dictionary of Scientific and Technical Terms.

Neither the specification nor the prosecution file history suggest that any meaning other than its ordinary meaning should apply to this phrase, and the Court will construe this claim phrase as follows:

"digital signal processing" means: extraction of information from digital signals, followed by analysis using various algorithms.

"digital signal computations"-claims 1 and 23

This phrase is found in claims 1 and 23 of the Garde patent. ADI originally proposed that this claim phrase should be construed as "computations specifically designed for implementing digital signal filters for processing audio or image data in real-time," citing Garde patent, 1:11-23. As before, ADI also cites to Motorola's website, as well as to definitions of three terms from the McGraw-Hill Dictionary of Scientific and Technical Terms (5th ed., 1994). In its letter to the Court of February 6, 2004, ADI modified its proposed construction for this term, offering the definition of "computations made by a special purpose digital computer in connection with real-time performance of highly numeric applications such as fast Fourier transforms, digital filters, image processing and speech recognition," again relying on Garde patent,

1:11-21. Motorola proposes that the disputed phrase should be construed as "operations on discrete and/or discontinuous signals," citing the 1996 IEEE Dictionary.

ADI's initially proposed construction appears to be unnecessarily limiting by reference to computations on specific types of data, and by requiring "real-time" operation. ADI's citations of support do not justify the proposed construction. ADI's modified proposal also requires "real-time" operation, and it requires that the computations be "made by a special purpose digital computer in connection with ... performance of highly numeric applications." While various of these requirements may be typical of digital signal computations, ADI cites no support for its position that the phrase is necessarily defined by these requirements.

The 1996 IEEE Dictionary definition provides an ordinary meaning for the phrase "digital signal." The Garde patent specification does not clearly define the phrase differently or compel any other meaning, and the prosecution history does not contain a clear disavowal of the ordinary meaning. The Court will construe this claim element as follows:

"digital signal computations" means: operations on discrete and/or discontinuous signals.

"instructions"-claims 1 and 20-23

This term is found in claims 1 and 20-23 of the Garde patent. ADI proposes that the word "instructions" should be construed as "members of a device's instruction set." Motorola proposes that the term should be construed as "a statement or expression consisting of an operation and its operands (if any), which can be interpreted by a [specified computation block] in order to perform some function or operation." Motorola cites the 1996 IEEE Dictionary, as well as the Garde patent, 15:4-6.

Generally speaking, an instruction may contain the operands, if any, upon which the function or operation will be performed, or it may contain an address or location of the operands. The specification of the Garde patent uses the term "instruction" consistently with this ordinarily understood meaning. For example, Figures 14A-14E illustrate different forms of instructions, and those instructions are described at 14:36-15:7. Nothing in the patent specification or the file history indicates that the term "instructions" should be given any meaning other than its commonly understood meaning.

ADI's proposed construction for the term "instructions" is not helpful in that it merely suggests that an "instruction" is one member of an "instruction set." Motorola's proposed construction deviates from the ordinary meaning by requiring that "specified computation blocks" must be involved in interpreting and executing the instruction. Neither the specification nor the file history mandates this requirement for an "instruction." The Court interprets this claim element as follows:

"instructions" means a statement or expression consisting of an operation and its operands (if any), which can be interpreted by a processor or computer in order to perform some function or operation."

"first subset of instructions/second subset of instructions"-claims 1 and 21-23

These phrases are found in claims 1 and 21-23 of the Garde patent. ADI proposes that these terms be construed to mean a first and second subset, respectively, of instructions, each of which is a member of the instruction set. Motorola proposes that the terms should mean a first part and a second part, respectively, of the instruction set that includes bit or bits that identify a first computation block and a second computation block, respectively, to which the instructions should be sent and the operations that the first and second

computation blocks should perform.

According to Webster's II New College Dictionary, 1995, a "subset" is "a mathematical set contained within a set." According to that same authority, a "set" is "a group of things of the same kind that belong together and are so used." An alternative definition for "set" is "a collection of distinct elements." Thus, the plain meaning of the phrase "first subset of said instructions" would be a first collection of instructions contained within the group of instructions. A "second subset of said instructions" would mean a second collection of instructions within the group of instructions. The phrase "said instructions" in these disputed phrases simply refers back to the "instructions" stored in the "memory," as referenced earlier in the claim. Nothing in the patent specification or in the prosecution file history suggests that these phrases have any meanings other than their ordinary meanings, nor is there any clear disavowal of the ordinary meanings of the phrases. The Court will construe these phrases according to their plain meanings, as follows:

"first subset of said instructions" means: first collection of instructions contained within the group of instructions referenced earlier in the claim, and

"second subset of instructions" means: second collection of instructions contained within the group of instructions referenced earlier in the claim.

"first and second subsets of said instructions are the same" / "first and second subsets of said instructions are different."-claims 21 and 22

The phrase "first and second subsets of said instructions are the same" is found in claim 21, and the phrase "first and second subsets of said instructions are different" is found in claim 22. ADI proposes that these phrases simply mean that the first subset of instructions and the second subset of instructions are the same and different, respectively. Motorola proposes that the first phrase means that the first subset of instructions and the second subset of instructions are identical and executed on both the first computation block and the second computation block, respectively. Motorola proposes that the second phrase means that the first subset of instructions and the second subset of instructions are not identical and the first subset of instructions is executed by the first computation block and the second subset of instructions is executed by the second computation block.

The 1995 Webster's II New College Dictionary defines "same" to mean "being the very one: identical." That same source defines "different" to mean "dissimilar in form, quality, amount, or nature: unlike." The specification imparts no special meaning to these phrases and the Prosecution history does not contain a clear disavowal of the plain and ordinary meaning. Therefore, the court interprets these claim elements as follows:

"first and second subsets of said instructions are the same" means: that the first subset of instructions is identical to the second subset of instructions.

"first and second subsets of said instructions are different" means: that the first subset of instructions is dissimilar to, or unlike, the second subset of instructions.

"Core Processor"-claim 1

The term "core processor" is found in claim 1 of the Garde patent. ADI argues that the term "core processor" refers to a processor that includes at least the elements recited in the claim (*e.g.*, a program

sequencer, and first and second computation blocks). ADI cites excerpts from the patent specification for support. Motorola proposes that the "core processor" is "a device that interprets and executes instructions, consisting of at least an instruction control unit and an arithmetic unit." Motorola cites to the 1996 IEEE Dictionary for support.

The definition offered by Motorola from the 1996 IEEE Dictionary is actually for the term "processor," rather than "core processor." The word "core" is defined as "the innermost or most important part: heart." Webster's II New College Dictionary (1995). The term "core processor" suggests something less than a "processor" as a whole.

The specification of the Garde patent does use the term "core processor," at column 2, lines 9-19, where it states:

The core processor comprises a program sequencer for generating instruction addresses for fetching selected ones of the instructions from the memory, a first computation block for performing a first subset of the digital signal computations under control of the program sequencer using a first subset of the instructions and a first subset of the operands, and a second computation block for performing a second subset of the digital signal computations under control of the program sequencer using a second subset of the instructions and a second subset of the operands.

The specification also states that the core processor is one component of the "digital signal processor," and the digital signal processor also includes a memory for storing instructions and operands, as well as "means for transferring" the first and second subsets of instructions and operands from the memory to the computation block. Thus, the "core processor" is only one component of the "digital signal processor."

Because the Garde patent specification expressly indicates what the core processor is, and because the definition contained in the 1996 IEEE Dictionary is for the term "processor" rather than "core processor," the Court will construe the term as follows:

"core processor" means: the portion of a digital signal processor that comprises a program sequencer for generating instruction addresses and first and second computation blocks for performing digital signal computations."

This interpretation of the phrase is also consistent with the language of claim 1 itself, wherein the core processor is specified as including a program sequencer and first and second computation blocks.

"program sequencer"-claim 1 and 23

The term "program sequencer" is found in claims 1 and 23 of the Garde patent. ADI has proposed that the "program sequencer" is "a device that determines the order in which instructions are to be fetched," citing to Figures 1 and 9 and an excerpt from the patent specification. Motorola proposes that the "program sequencer" is "a device that determines the order in which instructions are issued to computation block(s) and integer ALUs," also citing to Figure 9 and an excerpt from the patent specification.

Neither party submitted a dictionary definition for the disputed term. Rather, each party cites to 10:33-35 of the specification. In describing the disclosed embodiment, that excerpt states "the program sequencer 70 controls sequencing of instructions for the computation blocks 12 and 14 and for the integer ALU's 72 and

74." Elsewhere, the specification indicates that the program sequencer is "for generating instruction addresses for fetching selected ones of the instructions from the memory," and that the computation blocks perform digital signal computations "under control of the program sequencer." Gardepatent, 2:9-19. The specification also states that "the program sequencer 70 supplies a sequence of instruction addresses on one of the address buses 50, 52, 54 and 56, depending on the memory location of the instruction sequence." Garde patent, 4:52-55. Thus, the program sequencer in the disclosed embodiment is responsible "for generating instruction addresses for fetching ... instructions from the memory," and it also "controls sequencing of instructions for the computation blocks." Garde patent, 2:10-11; 10:33-34.

In its ordinary sense, the term "program sequencer" would refer to a device that determines the order of program instructions, without necessarily referring to the order of fetching program instructions or the order of issuing program instructions. In this particular case, however, the claims specify the function required of the "program sequencer"-"generating instruction addresses for fetching selected ones of said instructions from said memory." To require more of the program sequencer than is specified by the claims would require reading into the term "program sequencer" a function that is described for the disclosed embodiment in the specification. The Court will construe the term as follows:

"program sequencer" means: a device for generating instruction addresses for fetching instructions from the memory."

"under control of"-claims 1 and 23

This phrase is found in claims 1 and 23 of the Garde patent, and each of those claims specify that the first and second subsets of digital signal computations are performed "under control of" the program sequencer. ADI proposes that the phrase "under control of" be construed to mean "performing computations in accordance with the received instructions." Motorola proposes that the phrase should mean simply "at the direction of." Neither party cites to a dictionary, to the patent specification, or to the prosecution history for support.

According to Webster's II New College Dictionary, 1995, the word "under" may be understood in the context of the Garde patent to mean "subject to the authority, rule, or control of" or "subject to the supervision, instruction or influence of." The word "control" may also be understood, in the context of the Garde patent, to mean "authority or ability to regulate, direct, or influence." In describing the relationship between the program sequencer and the computation blocks, the Garde patent specification indicates that the first and second computation blocks perform the digital signal computations "under control of" the program sequencer. The program sequencer generates addresses for fetching instructions from the memory and controls sequencing of instructions for the computation blocks. Garde patent, 2:9-19; 10:32-35.

The Court will construe the disputed claim phrase as follows:

"under control of" means: subject to the supervision, influence or direction of.

"register file"-claim 1 and 23

The term "register file" is found in claims 1 and 23 of the Garde patent. ADI proposes that a "register file" is "a set of registers configured to store data temporarily." Motorola proposes that a "register file" is "a set of registers which may be addressed by their number in the set." Motorola cites the 1996 IEEE Dictionary, as well as an excerpt from the patent specification. ADI argues that its proposed construction is the "ordinary

meaning" of the phrase which is consistent with the use of the phrase in the patent specification.

The 1996 IEEE Dictionary defines a "register file" to be "a set of registers which may be addressed by their number in the set." The 1996 IEEE Dictionary defines "register memory" as "registers specifically included in the machine design for use as high-speed storage," a definition similar to that offered by ADI for the term "register file."

The patent specification uses the term "register file" in a manner consistent with the definition set forth in the 1996 IEEE Dictionary. Looking at Figure 2 of the patent, the registers appear to have alphanumeric names as opposed to simple numeric designations, however, it is clear from the specification and Figure 2 that the registers in the register file may be addressed by a designation. Also, in describing the disclosed embodiment, the specification indicates that destination and source registers may be specified by certain bits in an instruction and, hence, the registers can be "addressed," or designated. Garde patent, 8:41-48. The prosecution history of the Garde patent does not contain any clear disavowal of the ordinary meaning. The Court will construe the disputed phrase as follows:

"register file" means: a set of registers which may be addressed by their number or designation in the set.

"multiplier"-claims 1, 3, and 23

The term "multiplier" is found in claims 1,3 and 23 of the Garde patent. ADI proposes that a "multiplier" is "a device capable of performing multiplications." ADI did not discuss this term in its papers, nor did it cite to any support for its proposed construction. Motorola proposes that a "multiplier" is "a device that has two or more inputs and whose output is a representation of the product of the quantities represented by the input signals," citing the 1996 IEEE Dictionary.

The specification of the Garde patent uses the term "multiplier" in a manner consistent with the definition set forth in the 1996 IEEE Dictionary. In particular, the specification indicates that the multiplier performs multiplication operations (Garde patent, 2:30-31), and can selectively execute 32-bit by 32-bit multiplication instructions or quad 16-bit by 16-bit multiplication instructions (Garde patent, 2:34-37). The Court will construe this term as follows:

"multiplier" means: a device that has two or more inputs and whose output is a representation of the product of the quantities represented by the input signals.

"ALU"-claims 1 and 23

The "ALU" is an "arithmetic logic unit," and that phrase is found in claims 1 and 23 of the Garde patent. ADI proposes that an "ALU" is "a device that performs arithmetic and logical operations," citing an excerpt from the patent specification and the Encyclopedia of Electronics (2nd ed., 1990). Motorola proposes that an "ALU" is "a functional component of a computer system that performs arithmetic and logical operations and generating data addresses," citing the 1996 IEEE Dictionary, as well as Figures 1, 2 and 10 and an excerpt from the patent specification.

The 1996 IEEE Dictionary, under "arithmetic-logic unit," refers the reader to "arithmetic and logic unit." That source defines an "arithmetic and logic unit" to be "a functional component of a computer system that performs arithmetic and logical operations." The definition in the 1996 IEEE Dictionary does not specify that an "arithmetic and logic unit" generates data addresses. Motorola seeks to add this function to the

"ALU" based on a description in the specification of one function performed by certain of the ALUs in the disclosed embodiment.

The Garde patent specification uses the term "ALU" consistent with the definition of that term found in the 1996 IEEE Dictionary. Although certain of the ALUs in the embodiment described in the patent specification do generate addresses (see, 4:65-67), use of the ALU to perform this function is not inconsistent with the IEEE Dictionary definition inasmuch as the generation of data addresses would involve "arithmetic and logical operations." The specification does not plainly indicate that the term "ALU" should be understood to have a meaning different from its plain and ordinary meaning, nor does the prosecution file history contain a clear disavowal of the plain and ordinary meaning. The Court will construe this term as follows:

"ALU" means: a functional component of a computer system that performs arithmetic and logical operations.

"Means for transferring said first subset of said instructions and said first subset of said operands from said memory to said first computation block for execution and for transferring said second subset of said instructions and said second subset of said operands from said memory to said second computation block for execution"-Claim 1

This exact phrase is found in claim 1 of the Garde patent, while a similar phrase is found in claim 20. The phrase in claim 20 will be handled separately below. The parties agree that the "means" element in claim 1 should be construed under 35 U.S.C. s. 112, para. 6. The Court will first address construction of the functional recitation, as it appears in claim 1, and then will address what structure disclosed in the specification corresponds to the "means." Method claim 23 contains a very similar phrase, and the Court will address the use of the phrase in claim 23 below.

The functions recited in claim 1 for this "means" element are "transferring said first subset of said instructions and said first subset of said operands from said memory to said first computation block for execution and for transferring said second subset of said instructions and said subset of said operands from said memory to said second computation block for execution." With regard to the recited functions, ADI proposes that the phrase be construed to mean "transferring the first subset of instructions and operands from the memory to one of the computation blocks for execution, and transferring the second subset of instructions and operands from the memory to another computation block," citing two excerpts from the patent specification. Motorola proposes that the phrase should be construed to mean "transmitting the first subset of the instructions and the first subset of the operands from the memory via an instruction alignment buffer, a bus and a primary instruction decoder to the first computation block and transmitting the second subset of the instructions and the second subset of the operands from the memory via an instruction alignment buffer, a bus and a primary instruction decoder to the second computation block," also referring to an excerpt from the patent specification, as well as Figures 1 and 2 of the patent.

The word "transfer" means "to carry, remove, or shift from one position or place to another." Webster's II New College Dictionary, 1995. The Court has already construed the phrases "first subset of instructions" and "second subset of instructions." The parties did not dispute the meaning of the phrases "first subset of operands" and "second subset of operands." Thus, the plain meaning of the functional phrase under consideration would be "carrying, removing or shifting the first subset of instructions and first subset of operands from the memory to the first computation block for execution, and carrying, removing or shifting

the second subset of instructions and second subset of operands from the memory to the second computation block for execution."

The specification of the Garde patent uses the word "transfer" in its normal sense to mean that "data," which may represent instructions or operands, may be carried, removed or shifted from one location to another in the DSP. See, *e.g.,* Garde patent, 3:66-4:2; 4:24-35. The prosecution history of the Garde patent does not contain a clear disavowal of the plain meaning of this claim phrase.

The functional phrase of "transferring ..." itself does not specify the structure or structures by which the "transferring" is to take place. In other words, the functional phrase of "transferring ..." does not specify that the "transferring" is to be "via an instruction alignment buffer, a bus and a primary instruction decoder," as Motorola proposes. Even if those structures are properly included in a "means" for purposes of claim 1, the recitation of those structures in the functional phrase itself is inappropriate.

The Court will construe the phrase **"transferring said first subset of said instructions and said first subset of said operands from said memory to said first computation block for execution and for transferring said second subset of said instructions and said second subset of said operands from said memory to said second computation block for execution,"** in claim 1 to mean: carrying, removing or shifting the first subset of the instructions and the first subset of the operands from the memory to the first computation block for execution, and carrying, removing or shifting the second subset of the instructions and the second subset of the operands from the memory to the second computation block for execution.

Looking now to the **"means"** for performing the recited functions in claim 1, ADI proposes that the structures described in the specification for performing the recited functions are the data buses 60, 62 and 64, citing to excerpts from the patent specification. Motorola argues that the corresponding structures are an instruction alignment buffer, data buses and primary instruction decoder, also citing to excerpts from the patent specification, as well as to Figures 1, 2 and 14(a)-(e).

A structure disclosed in the specification is a part of the "means" structure only if the specification or prosecution history clearly links or associates that structure to the function(s) recited in the claim. B. Braun Med., Inc. v. Abbott Labs., 124 F.3d 1419 (Fed.Cir.1997).

ADI argues that the only structures that actually perform the function of "transferring" are the data buses 60, 62 and 64. According to ADI, the other structures proposed by Motorola-the instruction alignment buffer and the primary instruction decoder-perform functions other than "transferring." Motorola argues that the circuitry identified by the specification "that is necessary to transfer subsets of instructions and operands from the memory to the respective computation block(s)" are all of the components it has identified. According to Motorola, "without all of these components, the subsets of instructions would never traverse the path from the memory to the appropriate computation block(s)."

The Garde patent specification states:

The first address bus 50 and the first data bus 60 comprise a bus for transfer of data to and from memory bank 40. The second address bus 52 and the second data bus 62 comprise a second bus for transfer of data to and from memory bank 42. The third address bus 54 and the third data bus 64 comprise a third bus for transfer of data to and from memory bank 44.... As used herein, 'data' refers to binary words, which may represent either instructions or operands that are associated with the operation of the DSP 10.

Garde patent, 4:24-35. The specification also states:

The first, second and third memory banks are connected to the core processor by first, second and third data and address buses, respectively.

Garde patent, 2:46-48. At 3:66-4:2, the specification indicates:

The elements of the DSP 10 are interconnected by buses for efficient, high-speed operation. Each of the buses includes multiple lines for parallel transfer of binary information.

Each of these passages plainly indicates that each of the buses 60, 62 and 64 transfers "data," which may represent instructions or operands, between the memory banks and the computation blocks.

On the other hand, the specification indicates that the instruction alignment buffer performs the function of "aligning instructions that are read from memory on different clock cycles but are required to be executed in one clock cycle." Garde patent, 2:60-63. And the specification indicates that the primary instruction decoder "partially decode(s)" the instructions before they are transferred to the computation blocks. Garde patent, 2:63-67. Elsewhere, the specification states:

Instructions fetched from one of the memory banks 40, 42 and 44 are supplied to instruction alignment buffer 32 on one of the data buses 60, 62 and 64. The instructions are aligned for execution in the clock cycle required by the instruction sequence and are partially decoded by the primary instruction decoder 34.

Garde patent, 6:50-55. Again, in column 9, the patent specification indicates that when instructions are stored in memory without being aligned, "it is necessary to align the instructions for execution in the same clock cycle," and the specification refers again to the instruction alignment buffer 32. Garde patent, 9:55-62. At column 10, the specification describes in more detail the function being performed by the instruction alignment buffer, namely, aligning instructions that will be executed in a single clock cycle. The specification ends that particular description by stating that "the re aligned instruction line stored in instruction buffer 324 is supplied to primary instruction decoder 34 for partial decoding." Garde patent, 10:10-31. Thus, from the specification, it is plain that the instruction alignment buffer performs the function of aligning instructions, and the primary instruction decoder performs the function of partially decoding instructions.

The only structures disclosed in the specification that actually perform, and are clearly linked to, the function of "transferring" are each of the data buses 60, 62 and 64.

Thus, the court will construe **"means for transferring"** in claim 1 to include each of the data buses 60, 62 and 64, and equivalents thereof.

"means for transferring said instructions and operands from said memory to one or both of said first and second computation blocks"-Claim 20

This phrase is found in claim 20, which depends from claim 1. The parties agree this claim element is in "means plus function" form and should be construed under 35 U.S.C. s. 112, para. 6. ADI argues that the described structures that perform the recited function are the data buses 60, 62 and 64, again citing to

passages from the patent specification. Motorola argues that the disclosed structure that performs the recited function includes an instruction alignment buffer, data buses, primary instruction decoder and op code. Motorola also cites to excerpts from the patent specification, as well as to Figures 1, 2 and 14(a)-(e).

Because this is a "means plus function" element, the Court will first consider the function recited for this claim element. The function of this "means" element is "for transferring said instructions and operands from said memory to one or both of said first and second computation blocks during each clock cycle." This function is similar to that addressed above in connection with claim 1. The Court will construe this functional language to mean "carrying, removing or shifting instructions and operands from the memory to one of the first and second computation blocks or to both of the first and second computation blocks during each clock cycle." The Court has already defined the term "instructions," and the parties have agreed to the meanings of the terms "first computation block," "second computation block" and "during each clock cycle." The primary dispute in the case of this claim phrase regards what disclosed structure corresponds to the "means."

ADI argues that the disclosed structures are the data buses 60, 62 and 64, which are the same structures ADI pointed to for the "means for transferring" in claim 1. Motorola argues that the "means for transferring" in claim 20 cannot be the same as the "means for transferring" in claim 1 because the claim 1 "means for transferring" *includes* the claim 20 "means for transferring."

The function recited in claim 20 is more restrictive than the function recited for the "means for transferring" in claim 1. As described earlier, in claim 1, the "means for transferring" must simply transfer instructions and operands to the first computation block for execution and to the second computation block for execution. On the other hand, the "means for transferring" in claim 20 must transfer instructions and operands "to *one or both* of said first and second computation blocks," and it must do so "during each clock cycle." The specification describes the data buses 60, 62 and 64 as being connected between the memory banks 40, 42 and 44, respectively, and the first and second computation blocks 12 and 14. Given this three-bus arrangement, the patent specification states that "at least one instruction and two operands can be provided to computation blocks 12 and 14 in a single clock cycle." Garde patent, 4:37-39. Again, the specification indicates that "using quad word transfers, four instructions and eight operands, each of 32 bits, can be supplied to the computation blocks 12 and 14 in a single clock cycle." Garde patent, 5:33-35. Thus, the collection of buses 60, 62 and 64 performs the function of transferring data to one *or both* computation blocks during each clock cycle. This structure differs from that of the "means for transferring" in claim 1, which was each of buses 60, 62 and 64.

The additional structures advocated by Motorola as a part of the claim 20 "means for transferring" actually perform other functions, as described in connection with the claim 1 "means for transferring," and the Court will not include those structures in the claim 20 "means for transferring" for the same reasons.

The Court will construe the term in Claim 20 as follows:

"Means for transferring" are the collection of data buses 60, 62 and 64, and equivalents thereof.

"means for selectably executing"-Claim 3

This phrase is found in claim 3 of the Garde patent, and the parties agree that this claim element is written in "means plus function" form and should be construed under 35 U.S.C. s. 112, para. 6. ADI proposes that

this claim term be construed to be the multiplier/accumulator 120 and equivalents. Motorola argues that this claim element refers to undisclosed circuitry responsive to instructions that configures a multiplier for either a 32-bit by 32-bit operation or quad 16-bit operation. According to Motorola, because the patent specification fails to identify a corresponding structure, claim 3 is invalid under 35 U.S.C. s. 112, para. 2, as being indefinite.

Claim 3 depends from claim 1 and recites that "said multiplier includes means for selectably executing 32-bit by 32-bit multiplication instructions or quad 16-bit by 16-bit multiplication instructions." The function that is performed by this "means" claim element is that of "selectably executing 32-bit by 32-bit multiplication instructions or quad 16-bit by 16-bit multiplication instructions." ADI appears to place no particular emphasis on the word "selectably," whereas Motorola argues that the term "selectably" requires a selection and, thus, a configuration of the multiplier to execute the recited operations.

The patent specification states that the multiplier/accumulator 120 includes input registers 610 and 612, a multiplier 600, an output register 620 and an accumulator 630. The multiplier/ accumulator 120 supports a number of different operations, including 32-bit by 32-bit fixed point multiply or multiply-accumulate (MAC) and quad 16-bit fixed point MAC operations. According to the specification, "the multiplier 600 may be used as a 32-bit by 32-bit multiplier (FIG.12A) or as quad 16-bit by 16-bit multipliers 602, 604, 606 and 608 (FIGS. 12B and 12C)." Garde patent, 13:31-41. Although the phrase "selectably executing 32-bit by 32-bit multiplication instructions or quad 16-bit by 16-bit multiplication instructions" requires that a selection between the two operations be made, nothing in the claim requires that the subject "means" claim element perform the selection itself. Rather, the subject "means" claim element simply executes a selected operation, *i.e.,* 32-bit by 32-bit multiplication instructions or quad 16-bit by 16-bit multiplication instructions. The claim does not require a "configuring" function be performed by this "means" element.

However, as Motorola points out, claim 3 states that "said multiplier includes means for selectably executing," and construing the "means" to be the multiplier/accumulator 120 and equivalents essentially reduces claim 3 to reciting a multiplier that includes a multiplier. While the patent specification states that the multiplier/accumulator 120 supports various operations, including 32-bit by 32-bit multiply or MAC and quad 16-bit fixed point MAC operations, the specification states more specifically that the multiplier/accumulator 120 includes a number of components, including a multiplier 600. The specification states that "the multiplier 600 may be used as a 32-bit by 32-bit multiplier ... or as quad 16-bit by 16-bit multipliers 602, 604, 606 and 608." Hence, the structures disclosed in the patent specification for executing selected 32-bit by 32-bit multiplication instructions or quad 16-bit by 16-bit multiplication instructions are the multiplier 600 and multipliers 602, 604, 606 and 608. Therefore the Court will construe this term in Claim 3 as follows:

"means for selectably executing" are the multipliers 600, 602, 604, 606 and 608, and equivalents of that aggregate structure.

"transferring the first subset of the instructions and the first subset of the operands from the memory to the first computation block for execution and transferring the second subset of the instructions and the second subset of the operands from the memory to the second computation block for execution"- Claim 23

Motorola argues that this phrase from claim 23, a method claim, is in "step plus function" form, invoking 35 U.S.C. s. 112, para. 6. The preamble of claim 23 uses the familiar method-claiming phrase "comprising the

steps of." However, none of the individual limitations in the claim includes the phrase "step for." Hence, a rebuttable presumption arises that 35 U.S.C. s. 112, para. 6, does not apply.

The word "transferring" can be construed as an act, that is, some action to be taken in performing the claimed method. As the Court of Appeals for the Federal Circuit said in Masco Corp. v. U.S., 303 F.3d 1316,1327 (Fed.Cir.2002):

"Where the claim drafter has not signaled his intent to invoke Section 112, Paragraph 6, by using the 'step[s] for' language, we are unwilling to resort to that provision to constrain the scope of coverage of a claim limitation without a showing that the limitation contains nothing that can be construed as an act.... We thus hold that where a method does not contain the term 'step[s] for,' a limitation of that claim cannot be construed as a step-plus-function limitation without a showing that the limitation contains no act."

The Court finds that the phrase at issue is not in "step plus function" form, and the limitation should not be construed under 35 U.S.C. s. 112, para. 6. The Court will construe this phrase in the same way it construed the corresponding phrase from claim 1.

Therefore, **"transferring the first subset of the instructions and the first subset of the operands from the memory to the first computation block for execution and transferring the second subset of the instructions and the second subset of the operands from the memory to the second computation block for execution"** means: carrying, removing or shifting the first subset of the instructions and the first subset of the operands from the memory to the first computation block for execution, and carrying, removing or shifting the second subset of the instructions and the second subset of the operands from the memory to the second computation block for execution.

THE KATTMANN PATENT

U.S. Patent No. 5,175,550**,** the **Kattmann** Patent, is held by A.D.I. and was issued on December 29, 1992. The Kattmann Patent is entitled "Repetitive Cell Matching Technique for Integrated Circuits." It described an improvement relating to integrated circuits made with repetitive cells in which each cell is designed to be identical to all of the other cells. However, because manufacturing variations in the circuit elements can cause slight differences between the cells, the Kattmann Patent teaches the addition of an impedance network created by adding resistors between cells. These resistors divert a portion of the current flowing through any one cell into another cell or cells thereby reducing the magnitude of any error.

In the embodiment shown in Figure 1 of the Kattmann patent, each of the cells includes two transistors and two resistors Rl. Each resistor R1 is connected in series with one of the transistors, and the two resulting resistor/transistor series combinations are coupled together in parallel. A current source is connected to the two transistors. Each of the transistors receives an input signal at its base, and, depending upon the relative voltage levels of the two signals, one of the transistors will be turned on, allowing current to pass from the current source into the resistor that is connected to that transistor. However, manufacturing variations in the circuit elements that make up the cells cause slight differences between the cells, causing mismatch between the cells and resulting in errors.

A solution to cell mismatch and the resulting errors, according to the Kattmann patent, is the addition of an impedance network coupled to the repetitive cells. In particular, in the embodiment described in the Kattmann patent, two resistors R2 are connected between each pair of cells, as illustrated in Figure 1 of the

patent. The resistors R2 divert a portion of the current flowing through one cell into another cell or cells, thereby reducing the magnitude of any error.

Disputed Claim Terms of the Kattmann Patent

All claims of the Kattmann patent, claims 1-14, are at issue in this case, with claims 1, 5 and 12 being independent claims. Many of the disputed terms and phrases apply to multiple claims. Each claim term or phrase will be construed the same for purposes of each claim in which it appears.

For convenience, a copy of the patent page setting out the 14 claims is attached as Exhibit A on the following page.

EXHIBIT A

What is claimed is:

1. In a monolithic chip formed with an integrated circuit including a number of repetitive cells for producing output signals in response to respective inputs, each of said cells including a circuit element having two terminals to provide for the flow therethrough of a current from an associated current source and producing a corresponding cell output signal;

that improvement for reducing the effects of cell mismatch on said output signals comprising:

an impedance network comprising a set of impedance elements each connected between the corresponding terminals of respective pairs of said circuit elements, with each circuit element of such pairs forming part of a respective cell, said impedance elements permitting the flow of current therethrough serving to reduce the effects of cell mismatch on said output signals.

2. An integrated circuit as in claim 1, wherein said circuit elements for said cells have impedances in accordance with a predetermined pattern.

3. An integrated circuit as in claim 2, wherein said impedance elements have impedances in accordance with a predetermined pattern corresponding to said pattern of said circuit elements.

4. An integrated circuit as in claim 3, wherein said patterns of impedances provide equal-valued circuit elements and equal-valued impedance elements.

5. In a monolithic chip formed with an integrated circuit including a number of repetitive cells for producing output signals in response to respective inputs, each of said cells including a first resistor receiving a current from an associated current source and producing a corresponding cell output signal;

that improvement for reducing the effects of cell mismatch on said output signals comprising:

a resistor network comprising a set of second resistors each connected between the corresponding ends of respective pairs of said first resistors each forming part of a different cell, to permit the flow of current serving to reduce the effects of cell mismatch on said output signals.

6. An integrated circuit as in claim 5, wherein said first resistors for said cells have ohmic resistances in accordance with a predetermined pattern.

7. An integrated circuit as in claim 6 wherein said second resistors have ohmic resistances in accordance with a predetermined pattern corresponding to said pattern of said first resistors.

8. An integrated circuit as in claim 7, wherein said patterns of ohmic resistances provide equal-valued first resistors and equal-valued second resistors.

9. An integrated circuit as in claim 5, wherein each of said repetitive cells comprises a differential amplifier including a pair of transistors;

said first resistors being connected as pairs of resistors where one of each pair is in series with one of a corresponding pair of said transistors respectively to conduct current depending upon which transistor of the pair is turned on; and

a current source connected to both transistors of each pair to supply the current for the turned-on transistor.

10. An integrated circuit as in claim 9, wherein each of said differential amplifiers forms part of a comparator.

11. An integrated circuit as in claim 10, wherein said comparators are interconnected to form part of a flash-type A/D converter.

12. In a monolithic chip formed with an integrated circuit including a number of repetitive cells for producing output signals in response to respective inputs, each of said cells including a circuit element having two terminals to provide for the flow therethrough of a current from an associated current source and producing a corresponding cell output signal;

the method of reducing the effects of cell mismatch on said output signals comprising:

controllably diverting current between corresponding terminals of pairs of said circuit elements wherein each circuit element of such pairs forms part of a respective cell.

13. The method of claim 12, wherein said current is diverted between said corresponding terminals by respective impedance elements.

14. The method of claim 13, wherein said diverting is effected by resistors.

* * * * *

EXHIBIT A

"circuit element"-claim 1-4 and 12

ADI asserts that a "circuit element" is "an electronic component, such as a resistor, transistor, or capacitor, in a circuit." ADI points to the specification of the patent, as well as to the IEEE Standard Dictionary of Electrical and Electronics Terms (4th ed., 1988) defining the term "circuit" to mean "an interconnection of circuit elements." Motorola proposes that a "circuit element" be defined as "an impedance element," and

Motorola defines an "impedance element" to be "a device such as a resistor, inductor, or capacitor designed to provide impedance in an electric circuit." Motorola cites to the specification and to the McGraw-Hill Dictionary of Scientific and Technical Terms.

The plain meaning of the term "circuit element" would be an element, or component, of a circuit. As ADI points out, the word "circuit" means "an interconnection of circuit elements." Nothing in the term itself suggests that a "circuit element" must be "an impedance element" or any other particular type of circuit element.

Motorola points out that the specification consistently refers to "impedance circuit elements," and that the only type of circuit element in the cells that has two terminals to provide for the flow of a current are impedance elements, and, specifically, resistive elements. Motorola points out that the preamble of claim 1 of the Kattmann patent specifically states that the "circuit element" has "two terminals to provide for the flow therethrough of a current."

The ordinary meaning of the term "circuit element" does not limit the element to an impedance element or some other specific type of circuit element. Moreover, the passages in the specification on which Motorola relies refer to "impedance circuit elements" rather than simply "circuit elements," plainly suggesting there are "circuit elements" other than "impedance circuit elements." While the disclosed embodiment employs resistors, a form of "impedance circuit element," it would be improper to import that specific limitation into the claim language specifying simply a "circuit element." Nothing in the specification or the file history suggests that the term "circuit element" in itself, without any modifier, be limited to "an impedance circuit element." Accordingly, the Court will construe this disputed term as follows:

"circuit element" means: an electronic component, such as a resistor, transistor or capacitor, in a circuit,

"resistor"-claims 5, 6, 7, 8, and 9

Each of the parties has slightly modified its proposed definition for this term since the Markman hearing. ADI, in a letter of February 6, 2004, proposed that a "resistor" is "a device used in circuits that produces a voltage drop in response to an applied current," citing Merriam-Webster's New College Dictionary (1979). That source specifically defines a "resistor" to be "a device that has electrical resistance and that is used in an electric circuit for protection, operation, or current control." This is not a technical dictionary.

Motorola, in a letter of January 28, 2004, proposed that "resistor" be defined as "a device designed to have a specific range of resistance over its intended operating temperatures, used in circuits to limit current flow." Motorola had previously cited to the McGraw-Hill Dictionary of Scientific and Technical Terms (1989) to propose the definition "a device designed to have a definite amount of resistance, used in circuits to limit current flow or to provide a voltage drop."

ADI objects to Motorola's proposed definition for at least two reasons. First, ADI argues that "defining a 'resistor' in terms of providing a range of 'resistance' seems circular." Moreover, says ADI, a circuit element can be a resistor regardless of whether it was "designed" to have a "specific range of resistance," or whether it is being "used" by a circuit designer "to limit the current flow." Motorola argues that ADI's proposed definition reduces the "resistor" limitation to "a nullity." According to Motorola, ADI's definition would improperly read out of the claims a material limitation because, under ADI's definition, "the entire chip ... is a resistor."

Certainly a resistor is one particular type of a circuit element, and, in particular, a resistor is a circuit element that provides resistance to the flow of current in an electric circuit. See the dictionary sources cited by ADI and Motorola. However, as Motorola points out, such a definition offers little guidance as to the meaning of the term "resistor" as used in the Kattmann patent. The Court will construe this term as follows:

"resistor" means a device designed to have a definite, amount (which may be variable) of resistance, used in circuits to limit current flow or to provide a voltage drop. The amount of resistance be made to vary in a controlled fashion, as is in a variable resistor.

The first part of the definition is that found in the 1989 edition of the McGraw-Hill Dictionary of Scientific and Technical Terms, shortly before the filing date of the application leading to the Kattmannn patent, June 19, 1990. Nothing in the patent specification or the prosecution file history suggests the term "resistor" should have any special meaning aside from its ordinary meaning.

"cell mismatch"-claims 1 and 12

ADI proposes that "cell mismatch" be defined as "an output error caused by unmatched circuit elements within a repetitive cell or between two or more repetitive cells." Motorola proposes that the term be defined as "deviations from nominal in the value of a resistor, or in the output of a current source." Each of the parties cites various passages from the patent specification. In addition, ADI cites to the McGraw-Hill Dictionary of Scientific and Technical Terms (5th ed., 1994) which defines "mismatch" to be "the condition in which the impedance of a source does not match or equal the impedance of the connected load or transmission line." Neither party submitted a dictionary definition for the phrase "cell mismatch."

ADI argues that the Kattmann patent pertains to solving problems that arise when all of the repetitive cells are not identical, or when elements within a single repetitive cell do not match with one another. Although ADI cites to several passages in the specification, none support the view that the Kattmann patent is directed to solving problems that arise when elements within a repetitive cell do not match one another, apart from whether that particular cell matches the other repetitive cells in the integrated circuit. In fact, the term "cell mismatch" in itself suggests a mismatch between cells rather than a mismatch between components within a given cell.

Motorola's proposed definition, on the other hand, simply recites certain exemplary causes of cell mismatch, but those causes do not define the term "cell mismatch." See Kattmannn patent, 1:32-38. The Court will define this disputed term as follows:

"cell mismatch" means: a condition in which cells are not the same, resulting in an output error.

"associated current source"-claims 1 and 5

The preamble of claim 1 recites "each of said cells including a circuit element having two terminals to provide for the flow therethrough of a current from an associated current source." ADI proposes that the term "associated current source" should be defined as "a source of current connected to one of the repetitive cells." Motorola proposes that the term should be defined as "the current source within each repetitive cell." Each party cites to various passages in the specification.

Although neither party defined the word "associated," it means simply to unite in a relationship, or to

connect or join together. Webster's Second New College Dictionary (1995). Thus, a current source associated with a cell or associated with a circuit element in the cell would be a current source connected to, or joined to, that cell or circuit element. Nothing in the patent specification or file history suggests any other meaning should apply.

Motorola's proposed construction is flawed because it would apparently require that the current source be "within" a repetitive cell, whereas the plain meaning of the word "associated" only requires that the current source be connected to, but not necessarily within, a repetitive cell. Moreover, Motorola's proposed construction would appear to require that each repetitive cell have its own unique current source, and, although in the disclosed embodiment each repetitive cell appears to have its own current source, nothing in the specification or file history would dictate such an arrangement. The Court will construe this disputed phrase as follows:

"associated current source" means: a source of current connected to a repetitive cell.

"connected between the corresponding terminals of respective pairs of said circuit elements"-claims 1 and 12

Claim 1 calls for a set of impedance elements "each connected between the corresponding terminals of respective pairs of said circuit elements" in the cells. ADI proposes that the phrase "connected between the corresponding terminals of respective pairs of said circuit elements" means "an impedance element is connected between the corresponding terminals of two circuit elements each of which is located in a repetitive cell," citing Figure 1 and 3:54-66 of the patent specification. Motorola proposes that the phrase means "connected between corresponding ends of respective adjacent pairs of successive circuit elements," citing Figure 1, several excerpts from the patent specification, and a portion of the prosecution history from the Kattmann patent. The primary dispute between the parties lies in Motorola's proposed inclusion of the words "adjacent" and "successive" in its definition.

Motorola points to the embodiment described in the specification, and, in particular, to the connection of resistors R2 between resistors R1 and circuit elements that are next to each other in Fig. 1. Motorola argues that the patent does not disclose that including the resistors R2 in any other configuration results in the claimed improvement, and, therefore, does not support any broader interpretation. Motorola also points to the prosecution history of the Kattmann patent, and particularly to an amendment dated May 18, 1992. This amendment does not support Motorola's proposed construction. An argument made by the applicant in the referenced amendment states that the "impedance elements" of claim 1 read on the resistors R2 shown in Figures 1, 2 and 4 which "are connected between the cells." The applicant goes on to state that the resistors R2 shown in Figures 1 and 2 "are connected between corresponding ends of resistors R1 in adjacent cells 10A, 10B, etc. No such structure is shown in Laine." The mere fact that a claim term "reads on" a particular embodiment does not justify limiting that term to the particular embodiment. The argument by the applicant in the amendment distinguishes between resistors that are "between" cells and resistors that are located within a cell, as in Laine. Moreover, the argument contained in the amendment does not rise to the level of a "clear disavowal" needed to depart from the plain meaning of the claim language. The Court will construe this disputed phrase as follows:

"connected between the corresponding terminals of respective pairs of said circuit elements" means: connected between the corresponding terminals of two circuit elements, each of which is located in a repetitive cell.

"connected between the corresponding ends of respective pairs of said first resistors"-claim 5

This phrase appears in claim 5, and, for the reasons set forth above, the Court will construe this phrase to mean: **"connected between the corresponding ends of two other resistors, each of which is located in a repetitive cell."**

"between corresponding terminals of pairs of said circuit elements"-Claim 12

This phrase is found in claim 12, and, for the reasons set forth above, the Court will construe this phrase to mean: **between the corresponding terminals of two circuit elements, each of which is located in a repetitive cell.**

"equal valued"-claims 4 and 8

This phrase is found in claims 4 and 8 of the Kattmann patent. ADI proposes that the term should be construed as meaning "substantially equal value," citing several passages from the patent specification. Motorola proposes that the term be defined as "having the same impedance." Motorola also cites to the patent specification, as well as to the prosecution history, and specifically to an amendment dated January 9, 1992.

The plain meaning of the term "equal valued" would be "having the same value." The patent specification states that the "impedance (ohmic) values of the resistors R1 are in accordance with a predetermined pattern," and that "the resistors R1 are of equal ohmic value." Kattmann patent, 2:63-67. The specification also states that the "impedance (ohmic) values of the resistors R2 are in accordance with a predetermined pattern," and that, in the preferred embodiment described in the patent, "the ohmic resistances of the resistors R2 are all equal, as are the resistances of the resistors Rl." Kattmann patent, 3:58-64. These passages suggest that the plain meaning of "equal valued" is being used-that is, "having the same impedance (ohmic) value."

However, the specification also states that "in any practical implementation for an integrated circuit, there will be mismatches between the cells. Mismatch may result from a variety of causes, such as deviations from nominal in the value of a resistor Rl." Kattmann patent, 3:24-29. Hence, the specification recognizes that while two resistors such as resistors R1 may be of equal value nominally, deviations from those nominal values occur "in any practical implementation of an integrated circuit." Thus, in view of the specification taken as a whole, the phrase "equal valued" appears to mean "having the same nominal value."

In the prosecution history of the Kattmann patent, in an amendment A dated January 9, 1992, the applicant responded to the Examiner's position that the term "equal valued" has not been defined in the specification. The applicant referred to page 8, second paragraph, of the application (corresponding to 3:56-66 of the patent) as providing support for the claim term "equal valued." The Court has noted this passage from the patent specification, and, in view of the specification taken as a whole, and particularly in view of column 3, lines 27-29, the Court is of the opinion that the cited passage would be viewed by the person of ordinary skill in the art as plainly indicating that the nominal values of the resistors R1 and R2 in the preferred embodiment are equal. Accordingly, the Court will construe this disputed phase as follows:

"equal valued" in claims 4 and 8 means: having the same nominal value, in other words, designed to have the same value.

"first resistors being connected as pairs of resistors"-claim 9

ADI proposes that the phrase be construed to mean that each repetitive cell has a pair of resistors. Motorola proposes that the term be construed to mean that each repetitive cell has a pair of resistors connected to each other. Both parties cite to the patent specification.

In describing the disclosed embodiment, the patent specification states that "each cell includes a pair of resistors R1 which are connected together at their upper ends at a common point." Kattmann patent, 2:58-63. Claim 5, from which claim 9 depends, specifies that a set of second resistors is connected between "respective pairs of said first resistors." Thus, claim 5 requires "pairs of ... first resistors." Claim 9 then goes on to specify "said first resistors being connected as pairs of resistors." Separately, claim 9 calls for "a pair of transistors" as part of a differential amplifier, without specifying they are "connected as [a] pair." Hence, while the claim calls for a differential amplifier including "a pair of transistors," it does not simply call for "a pair of resistors." Rather, the claim calls for first resistors "being connected" as pairs of resistors.

ADI's proposed construction would effectively eliminate the "being connected" language from claim 9. ADI argues that the "being connected" language "refers to the pair of resistors that are connected to the pair of transistors in a repetitive cell." Analog's Opening Brief on Claim Construction for Analog's patents, p. 64. However, aside from the phrase "first resistors being connected as pairs of resistors," claim 9 goes on to state that "one of each pair is in series with one of a corresponding pair of said transistors respectively." Thus, while the claim does specify that each of the first resistors is in series with one of the pair of transistors, that limitation is separate and apart from the disputed phrase "first resistors being connected as pairs of resistors." The Court will construe this disputed phrase as follows:

"first resistors being connected as pairs of resistors" means: that each repetitive cell has a pair of resistors connected to each other.

"controllably diverting"-claim 12

ADI proposes that the phrase: controllably diverting" should be construed as meaning "diverting in a controlled fashion." Motorola argues that the claim term is not used in the specification and therefore is indefinite. But Motorola also argues that, if the Court finds the term to not be indefinite, it should be construed as meaning "diverting in a controllable fashion." At the Markman hearing, ADI's counsel conceded that, insofar as the proposed definitions are concerned, there is no difference between ADI's proposal and Motorola's proposal. Transcript, p. 353, 11.22-25.

The plain meaning of the phrase would appear to be "diverting in a controllable or controlled fashion." Motorola argues that each claim term must be sufficiently defined in the patent so as to be understood by one of ordinary skill in the art; otherwise the term is indefinite under 35 U.S.C. s. 112, para. 2. The phrase "controllably diverting" is not used in the specification of the Kattmann patent.

The fact that a word or phrase is not used in the patent specification does not mean that word or phrase cannot be properly construed. It is sufficient that a court can determine the meaning of the term or phrase from its plain meaning and the intrinsic record. In view of the essential agreement between the parties as to the plain meaning of the phrase, the fact that it is not used in the patent specification does not render the term indefinite. Indeed, the patent specification states that "if the cells are perfectly matched, the added network carries no current and thus has no effect on performance. If, however, elements of some of the

repetitive cells are imperfectly manufactured so as to create some degree of mismatch (as is often the case), the elements of the additional network carry corresponding currents which reduce the adverse effects of the mismatch on the device performance." Kattmann patent, 1:55-63. The specification also describes how the value of the R2 resistors affects the operation of the circuit. Kattmann patent, 4:26-5:28. Thus, the values of the resistors R1 and R2 may be controlled, and the "corresponding currents" that are carried by the elements of the additional network are thereby controlled. The Court will therefore construe the disputed phrase as follows:

"controllably diverting" means: diverting in a controllable or controlled fashion.

"diverted between said corresponding terminals"-claim 13

ADI proposes that the phrase "diverted between said corresponding terminals" means that the currents are diverted between the two terminals of one or more circuit elements. Motorola argues that the claim term is not used in the specification and is therefore indefinite. However, Motorola agrees that if the term is not found to be indefinite, ADI's proposed construction is the correct one.

The dispute between the parties is essentially the same as that involving the phrase "controllably diverting." For the reasons stated above, the Court will construe the disputed phrase as follows:

"diverted between said corresponding terminals" means: diverted between the two terminals of one or more circuit elements.

"is effected"-claim 14

Motorola argues that this phrase, found in claim 14, is indefinite, as it is not used in the patent specification. If the term is not found to be indefinite, says Motorola, it should be construed as meaning "caused." ADI agrees that the phrase means "caused." The Court will construe the disputed phrase according to its plain meaning as follows:

"is effected" means: is caused.

"current source"-claim 9

In the Joint Claim Construction chart submitted by the parties, the phrase "current source," appearing in claim 9, is indicated as being disputed. Although the parties' proposed constructions differ, the parties did not include arguments in their briefs concerning this claim phrase.

ADI proposes that the phrase be construed to mean "a circuit capable of supplying or sinking an electrical current." Motorola proposes the phrase be construed as meaning "a circuit capable of generating current to be supplied to both transistors."

Claim 9 provides that "a current source [is] connected to both transistors." Thus, the phrase "current source" need not include that the current source be "connected to both transistors," as that limitation is found in the claim apart from the phrase "current source."

Aside from this difference, the parties' proposed constructions are very similar. While ADI proposes that the current source is a circuit capable of "supplying or sinking" an electrical current, Motorola simply proposes

that the current source be a circuit capable of "generating current." Neither party has submitted any technical dictionary definition for the phrase, and the patent specification and prosecution history offer no guidance as to whether a "current source" should be capable of "supplying or sinking" an electrical current, or simply be capable of "generating current to be supplied." While the word "source" would ordinarily imply "supplying" as opposed to "sinking," there is nothing in the patent specification or otherwise to suggest that the direction of current flow generated by a "current source" must be into or out of the current source. As such, a circuit that "generates current" could presumably cause current to flow in either direction, In any event, the direction of current flow does not appear to be a point of contention. Hence, the Court will define this disputed term as follows:

"**current source**" means: a circuit capable of generating an electrical current.

THE MITCHELL AND BRANNICK PATENTS

United States Patent No. 6,230,119 B1**,** the **Mitchell** patent and United States Patent No. 6,289,300 B1**,** the **Brannick** patent, are held by ADI. The Court will address the Mitchell and Brannick patents together, as their specifications are substantially identical, their applications were filed on the same day, they are both assigned to ADI, and they share at least one claim term that is in dispute.

Both the Mitchell patent and the Brannick patent relate generally to a data processor having an embedded emulator that communicates with an external development system for purposes of debugging user code. Generally speaking, the Brannick patent concerns the data processor with an embedded debugger, while the Mitchell patent is concerned with the interface between the embedded emulator and an external development system. In Brannick, the data processor can be operated in first and second modes, In the first mode, the processor executes the user program, and in the second mode, the data processor operates to, for example, debug the user code. In performing a debugging operation, the data processor executes code stored in an emulation memory. In the Mitchell patent, the emulator in the data processor performs bi-directional communication with the external development system by way of only a single terminal.

The parties have agreed to the construction of most of the terms in the asserted claims. Claim 1 is the only asserted claim from the Mitchell patent. Claims 33, 36, 38, 39, 40, 43, 44, 47, 50 and 51-54, set out below, are asserted from the Brannick patent.

33. An integrated circuit comprising **a data processor** operable in a first mode to execute a user's program and in a second mode to **debug** the user's program and in which the data processor executes code stored in an emulation memory when the data processor is operating in the second mode.

36. A **data processor** operable in a first mode to execute user code stored in a **non-volatile user code memory** and in a second mode to execute code stored in an internal reserved memory, wherein the user code is re-programmable while the data processor is in the second mode and in the second mode, the data processor **acts to allow the user code to be debugged.**

44. A data processor operable in a first mode to execute the user code from an integrated memory, and in a second mode to execute debug code stored in an integrated non-volatile reserved memory; in which in the second mode the data processor executes instructions to communicate its internal status to an external development system and receive data and command information from the development system, where said **communication is bi-directional** via only a single terminal.

47. A **data processor** according to claim 44, in which the reserved memory **is hidden from the user.**

54. A method of debugging a **data processor** wherein the **data processor** is operable in a first mode to execute user code from an integrated memory, and in a second mode to execute debug code stored in reserved integrated memory; and in which in the second mode the data processor executes instructions to communicate its internal status to an external development system, and receive data and command information from the development system, where said **communication is bi-directional** via only a single terminal.

"data processor"-Mitchell Claim 1 and Brannick Claims 33, 36, 38, 39, 40, 43, 44, 47-49, 51-54.

The term "data processor" appears in the asserted claims of both the Brannick and Mitchell patents, In claim 1 of the Mitchell patent, the term appears only in the preamble. In each case, ADI proposes that a "data processor" is "a digital electronic processor containing non-volatile memory that is reprogrammable," referring to several excerpts from the patent specifications. Motorola proposes that a "data processor" is "a processor capable of performing operations on data. For example: a desk calculator or tabulating machine, or a computer." Motorola cites to the 2000 IEEE Dictionary for support. The applications leading to the Brannick and Mitchell patents were filed in 1998, and both patents issued in 2001.

Although the definition proposed by Motorola comes from the 2000 IEEE Dictionary, FN1 ADI argues that the definition is simply too broad and generic and can be used to describe many things, including, a human being. Thus, says ADI, the Court should look to the specification to construe the term in view of a proper context. ADI relies on the specification to argue that the "data processor" must contain non-volatile memory that is reprogrammable. However, the citations provided by ADI do not support ADI's proposed construction. For example, the citations indicate that "a reserve non-volatile memory" may be "advantageously" used and that "preferably" the emulation instructions may be held within a reserve memory. Brannick patent, 2:14-17 and 58-60. ADI also points to the disclosed embodiment where the data processor includes a non-volatile memory that is reprogrammable. However, these passages from the specification do not mandate a construction of the term "data processor" that includes a "non-volatile memory that is reprogrammable."

FN1. At the hearing, Motorola argued that the identical definition was also found in the 1994 IEEE Dictionary.

ADI argues that the claimed invention in Brannick "has a specific purpose, *i.e.*, to combine other debugging functions with reprogramming of reprogrammable non-volatile memory in a single emulation mode of a data processor." Although the invention may have a particular purpose, such a purpose does not justify a special definition for this term. ADI also points to specific requirements in other claims to support its position that the data processor must contain reprogrammable non volatile memory. These requirements in other claims also do not dictate a special meaning for the term "data processor."

The definition for a "data processor" taken from the 2000 IEEE Dictionary, a processor capable of performing operations on data, is an appropriate starting point in construing this phrase. A "processor," as defined by the 1996 IEEE Dictionary, is "a device that interprets and executes instructions, consisting of at least an instruction control unit and an arithmetic unit." FN2 In looking to the specification, the Court finds

no definition for the term clearly set forth that differs from those contained in the 1996 and 200 IEEE Dictionaries. The specification uses the phrase "data processor" in a manner that is consistent with the definitions found in those dictionaries. Moreover, ADI has pointed to nothing in the prosecution file history that would constitute a clear disavowal of the plain meaning of the phrase "data processor." At the hearing on January 22, 2004, ADI conceded that the specification did not include such a clearly set forth definition and that the prosecution history did not contain a clear disavowal. See Hearing Tr., pp. 292-93. Instead, ADI argues that the specification should be used to more specifically define a term which ADI argues is too broad and generic.

FN2. This excerpt from the 1996 IEEE Dictionary was submitted as Exhibit 6H to Motorola's Response to Analog's Opening Brief on Claim Construction for Analog's Patents. Both the Brannick and Mitchell patents were filed February 6, 1998.

Although the specification indicates that the data processor includes an emulator and memory, and it indicates that the memory may include a user code space and an emulation space, nothing in the specification suggests that the term "data processor" itself should be understood to mean anything other than what it would plainly and ordinarily mean. In the context of the claims of the Brannick and Mitchell patents, it will be understood that a "data processor," with the recited components and capabilities, would not encompass a human being. And the definition of "processor" reinforces that fact. Nothing in the specification dictates a special meaning for the term, and the prosecution history does not contain a clear disavowal of its ordinary meaning.

Therefore, the Court will construe the term **"data processor,"** for purposes of the Brannick and Mitchell "patents, to mean "a processor capable of performing operations on data." The term **"processor"** will be construed to mean "a device that interprets and executes instructions, consisting of at least an instruction control unit and an arithmetic unit."

"bi-directional communication"-Mitchell, claim 1

This phrase is found in claim 1 of the Mitchell patent. Although the meaning of this term was originally disputed, at the hearing on January 22, 2004, the parties agreed to the following construction: "information, including register values, as communicated from the emulator to the external development system and information, including break point instructions, as communicated from the external development system to the emulator." See Hearing Tr., p. 297, ll. 5-8.

"non-volatile user code memory"-Brannick, claim 36

This phrase is found in claim 36 of the Brannick patent. ADI proposes that the phrase means "non-volatile programmable memory for storing user code," citing passages from the Brannick patent specification. Motorola proposes that the term means "a non-volatile memory that stores the user's software instructions .... on-volatile memory is memory whose contents are retained when power is no longer supplied." Motorola cites a passage from the patent specification, as well as the 2000 IEEE Dictionary.

The parties are generally in agreement with respect to the construction of this phrase, with the exception that ADI contends that the non-volatile memory must be "programmable." In its paper, ADI argues that the non-volatile memory must be "reprogrammable," because claim 36 later recites that the user code, stored in the non-volatile user code memory, be reprogrammable. However, the presence of this additional limitation in

later claims does not justify deviating from the plain meaning of the phrase "non-volatile user code memory." While the user code memory in the disclosed embodiment of the patent specification may be reprogrammable, nothing in the specification indicates that a "non-volatile user code memory," in and of itself, is necessarily reprogrammable.

The parties agree that the "non-volatile user code memory" is a non-volatile memory that stores the user code. The parties also agree that a non-volatile memory is a memory whose contents are retained when power is no longer supplied. See, Analog's Opening Brief on Claim Construction for Analog's Patents, p. 40. Thus, the Court will construe the disputed phrash as follows:

"non-volatile user code memory" means a memory that stores user programming, where the memory's contents are retained when power is no longer supplied to the memory.

"hidden from the user"-Brannick claims 38 and 47

The phrase **"hidden from the user"** is found in claims 38 and 47 of the Brannick patent. ADI initially proposed that this phrase should be interpreted as "not used in the first mode," citing various excerpts from the patent specification. ADI later offered an alternative proposed construction as a compromise between the parties, and ADI is currently proposing that the phrase "hidden from the user" be construed to mean "not generally accessible to or intended for routine use by an end user." Motorola has rejected that proposal and argues that the phrase should be construed to mean "the reserve memory 'is placed on another page of memory,' which is not accessible or visible to the user in the first mode." Motorola cites to a passage from the patent specification for support.

Claim 38 indicates that the reserve memory is "hidden from the user." The parties appear to agree that the disputed phrase connotes at least a certain level of inaccessibility by the user. The primary difference between the parties' proposed constructions is that Motorola proposes that the construction include a description of one particular way of rendering the reserve memory inaccessible, namely, by placing the reserve memory "on another page of memory." FN3

FN3. The parties also originally differed in proposed constructions in that ADI simply proposed that the reserved memory is "not used" in the first mode. ADI has modified that position, as noted. Letters from ADI counsel dated February 6, 2004 and March 11, 2004.

The plain meaning of the phrase "hidden from the user" is "not accessible by or visible to the user." While Motorola points to an argument made during the prosecution of claim 38, that argument does not amount of a clear disavowal of the plain meaning of the phrase. Rather, the argument made during the prosecution was simply that the disclosure of Figure 3A supports claim 38, a statement that was made inasmuch as claim 38 was added during the prosecution of the patent application. The Court will not interpret that phrase to mean that the phrase "hidden from the user" will be limited to what is shown in Figure 3A. On the other hand, ADI argues that the phrase should simply mean not "generally" accessible to or intended for "routine" use by an end user. The language of the claim is clear, in that it requires that the reserve memory is "hidden from the user." The Court will interpret the disputed phrase as follows:

"hidden from the user" means not accessible by, or visible to, the user.

"communication is bi-directional"-Brannick claims 44 and 54

The phrase **"communication is bi-directional"** found in claims 44 and 54 of the Brannick patent is very similar to a phrase discussed earlier-"bi-directional communication." ADI proposes that this phrase be construed to mean "information that is communicated from the data processor to the external development system and from the external development system to the data processor." Motorola argues that the phrase should be construed to mean "the communication referred to above can travel in both directions-from the data processor to the emulator and from the emulator to the data processor. The data processor must have the ability both to insert breakpoint instructions and to read register values." Motorola contends that this phrase is substantially identical to the term "bi-directional communication" in the Mitchell patent, and it should be interpreted in the same way that phrase was interpreted.

The phrases in the Brannick claims and Mitchell claims are different, and the asserted claims in those patents are substantially different. The two patents are not related in the sense of one being a continuation or divisional from the other. Although the specifications are very similar, the claimed subject matter is different between the two patents. Each of claims 44 and 54 of the Brannick patent expressly describe communication between the data processor and the external development system when the data processor is operating in the second mode. Each claim then goes on to recite that "said communication" is bi-directional. The plain meaning of this phrase is that the "communication" specifically recited in the claims is "bi-directional," that is, in two directions. The specification of the Brannick patent uses the term "bi-directional" in a manner consistent with its ordinary meaning of "in two directions." Brannick patent, 3:19-38. Nothing in the prosecution history of the Brannick patent suggests a clear disavowal of the plain meaning of the phrase. Motorola has offered no legal support for its argument that the argument made in the Mitchell prosecution history should affect the meaning of this phrase in the Brannick patent. The Court will construe the disputed phrase as follows:

"communication is bi-directional" means: the communication is in two directions, from the data processor to the external development system and from the external development system to the data processor.

Other Terms from the Mitchell and Brannick Patents

The parties previously disputed additional terms from the Mitchell and Brannick patent claims, but, at the hearing on January 22, 2004, the parties announced agreement on those terms.

The parties have agreed that the phrase **"acts to allow the user code to be debugged"** in claim 36 of the Brannick patent should be construed to mean "when in the second mode, the data processor functions so as to permit the user software to be debugged." Hearing Tr., p. 284, and letters from counsel of February 6 and February 11, 2004.

The parties have agreed that the term **"debug"** in claim 33 of the Brannick patent should be construed to mean "to detect, locate, and correct faults in a computer program." Hearing Tr., pp. 284-85.

THE REMEDI PATENT

United States Patent No. 4,758,945**,** the **Remedi** patent is held by Motorola and was issued on July 19, 1988. The Remedi patent involves a method of reducing the power that is consumed by a microprocessor. A microprocessor is a digital logic device, and digital logic devices generally require a master clock signal to synchronize their internal circuitry. Remedi patent, 1:52-54. This master clock acts like a metronome,

providing a regular beat that the many circuit components of the device use to stay in time with each other as they perform their respective functions. The master clock, usually an "oscillator," generates an oscillating, or regular up and down, signal. Although the master clock is essential for maintaining proper synchronization of circuits, it consumes energy whenever it is oscillating. In addition, the passage of the clock signals throughout the device consumes energy, due to repeatedly charging and discharging of the circuit's components and because of stray capacitances in the many wires in the device.

The Remedi patent teaches a method of reducing power usage by stopping the clock oscillations when the device is not being used. When the device is needed again, signals are inhibited until the oscillator is "warmed up" and giving the proper signals.

Claims 1-6 of the Remedi patent are at issue in this case. The parties dispute the meaning of several claim terms found in claims 1 and 4, the two independent claims which are set out below.

1. In a digital computing system which executes **software instructions** in synchronization with **clock signals generated by a master clock oscillator** in an **enabled condition** thereof, a method for reducing the energy consumed by the digital system, comprising the steps of: decoding a **predetermined software instruction** selected for execution by said digital computing system; inhibiting passage of said clock signals from said master clock oscillator to said digital computing system in response to the decoding of said **predetermined software instructions,** and continuing to inhibit passage of said clock signals for a predetermined length of time after said master clock oscillator has been enabled; disabling the **generation of** said clock signals by said master clock oscillator in response to the **decoding** of said predetermined software instruction; and **enabling the generation of said clock signals by said master clock oscillator** in response to a control signal.

4. In a digital computing system which executes **software instructions** in synchronization with **clock signals generated by a master clock oscillaator** in an **enabled condition** thereof, a method for reducing the energy consumed by the digital system, comprising the steps of: executing a **predetermined software instruction** selected for execution by said digital computing system; inhibiting passage of said clock signals from said master clock oscillator to said digital computing system in response to the execution of said predetermined software instruction, and continuing to inhibit passage of said clock signals for a predetermined length of time after said master clock oscillator has been **enabled;** disabling the **generation of** said clock signals by said master clock oscillator in response to the **decoding** of said predetermined software instruction; and **enabling the generation of said clock signals by said master clock oscillator** in response to a control signal.

"clock signals"-claims 1 and 4

Motorola proposes that the phrase "clock signals" means "electronic pulses which are emitted periodically, usually by a crystal device, to synchronize the operation of circuits in a computer," citing McGraw-Hill Dictionary of Scientific and Technical Terms, 4th ed., 1989, as well as to several passages from the patent specification. ADI proposes that the phrase means "i.) clock signal; an oscillatory signal that is generated by the master clock oscillator and applied to some or all of the components in the digital computing system for controlling synchronization of the components, ii.) clock signals: more than one clock signal." ADI cites to the patent specification as well as to the prosecution history. The primary dispute between the parties on this claim term appears to be whether the terms "clock signals" and "clock pulses" have the same or different meanings, that is, whether a single clock pulse can be considered a "clock signal.".

The dictionary on which Motorola relies is dated the year following the issuance of the Remedi patent and is therefore relatively contemporaneous with the issuance of the patent. That dictionary's entry for "clock signals" refers the reader to the term "clock pulses." In the definition of "clock pulses," the dictionary states, "also known as clock signals." These two entries suggest that the two terms are interchangeable or synonymous. The definition set forth in this dictionary for the term "clock pulses" is that proposed by Motorola for the term "clock signals."

Both terms, "clock signals" and "clock pulses," are used in the specification of the Remedi patent. Terms in the claim of a patent should be interpreted consistently with their usage in the specification. As Motorola argues, and consistent with the dictionary source cited by Motorola, the specification of the Remedi patent appears to use the two terms, "clock signals" and "clock pulses," interchangeably. For example, in describing what is shown in Figure 4 of the patent, the specification refers to "C1 and C2" as "first and second clock signals." Remedi patent, 6:41, 7:25-26. Later in the same paragraph, the specification refers to "clock pulses C1 and C2." Remedi patent, 6:56. The specification again refers to "clock signals C1 and C2," then shortly thereafter refers to "clock pulses C1 and C2." Remedi patent, 8:17 and 8:43. Also, the specification refers to "clock pulse C2" and "this clock signal," both referring to C2. Remedi patent, 7:13-14. Thus, the specification refers to outputs in Figure 4 designated C1 and C2 as both "clock signals" and "clock pulses." Moreover, the specification refers to one of those outputs, C2, as both a "clock pulse" and a "clock signal." Remedi patent, 7:13-14, 8:58. One other example from the patent specification further illustrates that the Remedi patent uses the terms "clock signal" and "clock pulse" interchangeably. At column 7, lines 21-22, the specification refers to "the next clock signal appearing on output 116," while at column 8, line 39, the specification states that "the next pulse occurs on output 116." In fact, the Remedi patent specification uses the term "clock signal" to refer to one edge of one clock pulse. See 7:21-22.

By letter of February 6, 2004, ADI submitted supplemental evidence in support of its position. That extrinsic evidence relates to the term "clock" and does not plainly establish a difference between the terms "clock signal" and "clock pulse."

The Court finds that the Remedi patent uses the terms "clock signals" and "clock pulses" interchangeably to refer to the same things. Moreover, the Court finds that the Remedi patent uses the phrase "clock signal" interchangeably with the phrase "clock pulse." Thus, just as the definition contained in the McGraw-Hill Dictionary of Scientific and Technical Terms indicate that the terms "clock signals" and "clock pulses" are interchangeable, the Remedi patent specification also uses those terms interchangeably. Nothing in the intrinsic record suggests the two terms should have different meanings. Consequently, the Court interprets the disputed phrase as follows:

"clock signals" means electronic pulses which are emitted periodically, usually by a crystal device, to synchronize the operation of circuits in a computer.

"spftware instruction(s)"-claims 1 and 4

Motorola proposes that the term "software instruction" means "a software statement that specifies an operation and the values or locations or its operands," citing the IEEE Dictionary of 1977. ADI proposes that the phrase "software instruction" means "i. the set of instructions that a processor is capable of executing, ii. a 'software instruction' is a member of this set." ADI cites to the definition of the phrase "instruction set" taken from the Free On-line Dictionary of Computing. ADI also points to the Remedi

patent specification, at 5:25-44, where the "instruction repertoire," or instruction set, is mentioned. ADI also argues that Motorola explained during prosecution that the "STOP and WAIT instructions are new instructions which are added to the repertoire of instructions already available to the user."

The dictionary definition cited by ADI, as well as the citations to the specification and to the prosecution history, relate to the "instruction set" of a processor. However, the term at issue is "software instructions." ADI offers no support for its position that the term "software instructions" should be defined as a complete instruction set as opposed to the more generic definition contained in the IEEE dictionary cited by Motorola. The intrinsic record does not indicate that the applicant intended to use the phrase "software instruction" or "software instructions" to have any meaning other than its ordinary meaning. The specification contains no clear indication of a special meaning, nor does the prosecution history contain a clear disavowal of the ordinary meaning of the phrase.

The Court finds that the phrase **"software instruction"** means "a software statement that specifies an operation and the values or locations of its operands." The Court finds that the phrase **"software instructions"** means "more than one software instruction."

"generated by/generation of"-claims 1 and 4

While these phrases were initially disputed, the parties have now agreed that, for purposes of the Remedi patent, the phrase **"generated by"** means "produced by," and that the phrase **"generation of"** means "production of."

"master clock oscillator"-claims 1 and 4

This claim term was also initially disputed, but the parties have since reached agreement on its meaning for purposes of the Remedi patent. The parties have agreed that the term **"master clock oscillator"** means "the electronic or electric source of standard timing signals required for the execution of instructions in the operation of a computer."

"enabled condition/enabled"-claims 1 and 4

The meanings of these terms were also initially disputed, but the parties have since agreed that the meaning of the term **"enabled"** and the phrase **"enabled condition"** is "turned on." The Court also finds that the term **"enabling,"** also found in the claims, means "turning on."

"enabling the generation of said clock signals by said master clock oscillator"-claims 1 and 4

The Court finds that each of the terms in this phrase has been agreed to by the parties or defined by the Court, and no further construction of this phrase is needed. Specifically, the parties have agreed to the definitions of **"enabling," "generation of,"** and **"master clock oscillator."** The Court has defined the term **"clock signals."**

"predetermined software instruction"-claims 1 and 4

Motorola contend that this phrase should be interpreted as "a software instruction determined beforehand," citing Webster's New Collegiate Dictionary, 1974, defining the word "predetermined." ADI proposes that the phrase "predetermined software instruction" means "a member of the instruction set, the execution of

which always produces the same effect." ADI agrees that the word "predetermined" is defined in Webster's New World College Dictionary as "to determine, decide or decree beforehand."

The Court has now construed the term "software instruction" above, and the parties agree that the word "predetermined" simply means "to determine beforehand." Thus, the Court finds that the term **"predetermined software instruction"** means: a software instruction, as previously defined by the Court, determined beforehand.

"decoding."-claim 4

This term appears in both claims 1 and 4 of the Remedi patent. The parties agree that the word "decoding," as it appears in claim 1, means "interpreting the bits of a machine language instruction." However, there is a dispute concerning this word as it appears in claim 4.

The parties do not dispute what definition should apply to the word "decoding" in claim 4. Rather, ADI argues that the word is indefinite, rendering claim 4 invalid under 35 U.S.C. s. 112, para. 2, because of the use of the article "the" without establishing an antecedent basis for the term in the claim. Motorola contends that the word "decoding" in claim 4 is an error and should be understood to be "execution."

Motorola, in support of its position, points to the prosecution history of the Remedi patent where the applicants added a second set of claims substantially identical to the first set, except that the word "decoding" in the first and second paragraphs of the first claim set would be changed to "executing." Motorola argues in its claim construction brief that the applicant "also intended to change the word 'decoding' in the *third* subparagraph to 'execution.' " Motorola also argues that "it is readily apparent to any reader of the file history" that the applicant intended to replace the word "decoding" in the third paragraph of issued claim 4 with the word "execution."

The Court does not agree with Motorola's characterization of the file history. The applicants plainly indicated to the Examiner that new application claim 10 (issued claim 4) was to be identical to application claim 6 (issued claim 1), "except that the word 'decoding' in the first and second paragraphs of claim 6 would be changed to 'executing.' " The applicants did not indicate to the Examiner that they intended to change the word "decoding" in the third paragraph of claim 6 to the word "executing." Although the applicants did state that "this change is intended to clearly indicate that it is immaterial whether the present invention is characterized as being responsive to the 'decoding' or to the 'executing' of the 'predetermined instruction,' " the second paragraph of issued claim 4 does indicate that "inhibiting passage" is in response to the "execution of said predetermined software instruction." Hence, this difference between application claims 6 and 10 in their second paragraphs is consistent with the applicants' statements to the Examiner.

The Court also does not agree with ADI's position that the use of the term "the decoding" in claim 4 renders the claim indefinite and invalid under s. 112, para. 2. While it is true that the use of the article "the" before a limitation in a claim typically signals that the limitation has been previously set forth in the claim, the relevant inquiry is whether the meaning of the claim would be clear to the person of ordinary skill in the art. The Court finds that one of ordinary skill in the art would know that a software instruction is commonly decoded before being useful in "a digital computing system." Thus, reference to "the" decoding of a software instruction, without a previous reference to the word "decoding" in the claim does not render the claim indefinite and invalid.

The Court declines Motorola's invitation to rewrite claim 4, and particularly the third paragraph of claim 4, to replace the word "decoding" with the word "executing." The Court finds no ambiguity in the claim as issued, and the parties have previously agreed as to the definition of the word "decoding" as it is used in claim 1 of the Remedi patent. Accordingly, the court interprets this disputed term in claim 4 in the same way it is used in claim 1, namely:

"**decoding**" means: interpreting the bits of a machine language instruction.

CONCLUSION

The jury should be instructed in accordance with the court's interpretation of the disputed claim terms in the Garde, Kattmann, Brannick, Mitchell, and Remedi patents.

Signed June *5,* 2004.

E.D.Tex.,2004.
Motorola, Inc. v. Analog Devices, Inc.

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